

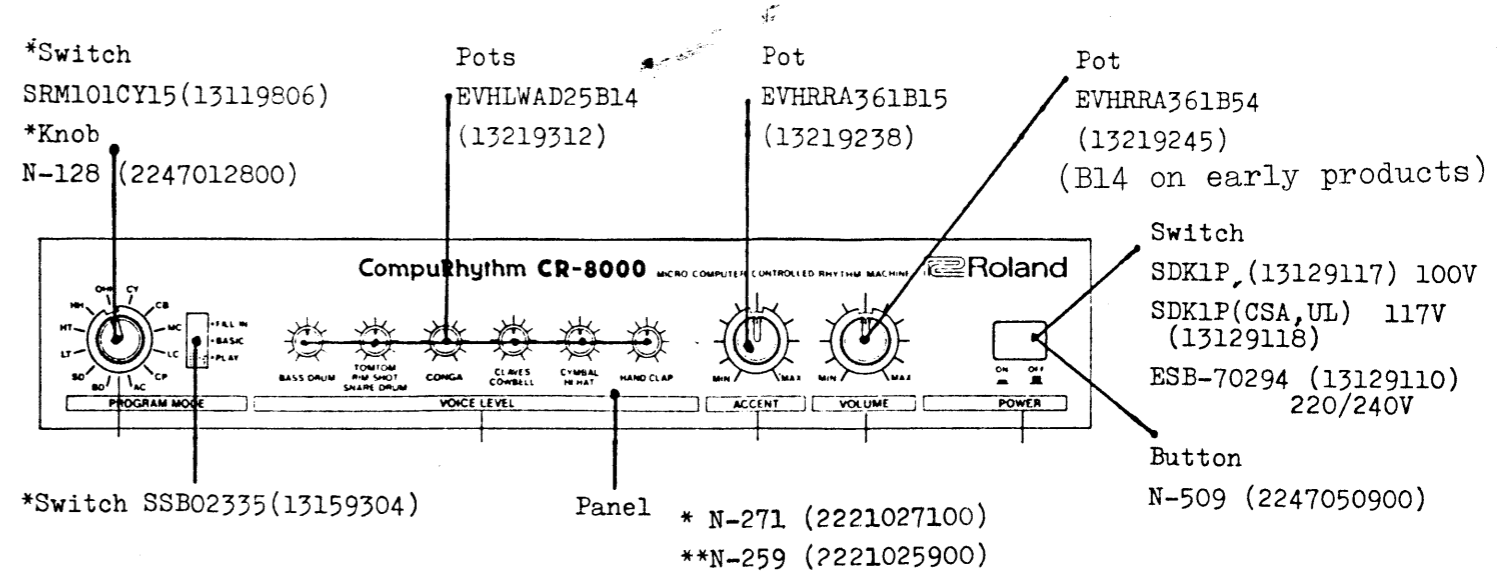
# CR-5000/8000 SERVICE NOTES

## SPECIFICATIONS

*First Edition*

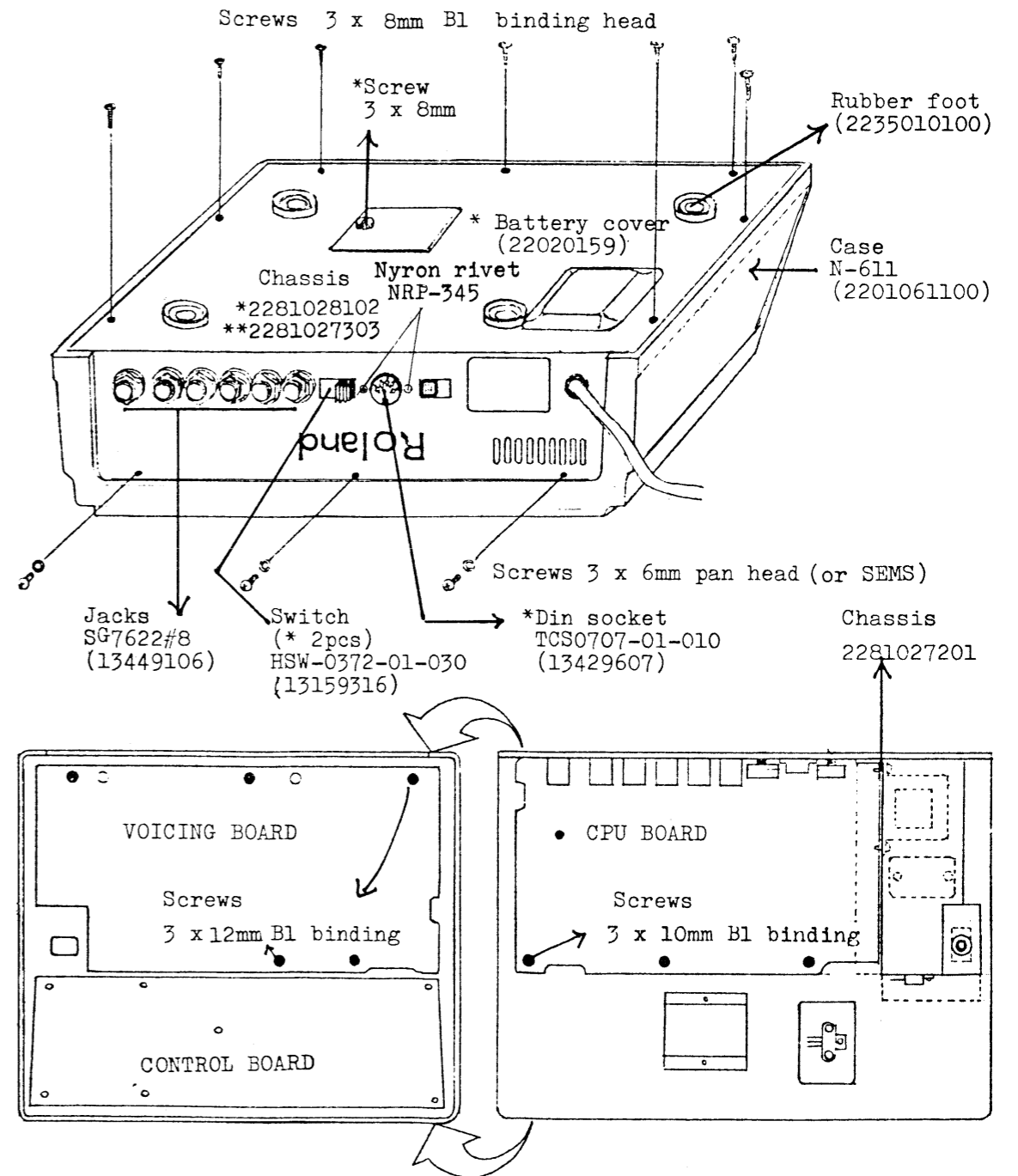
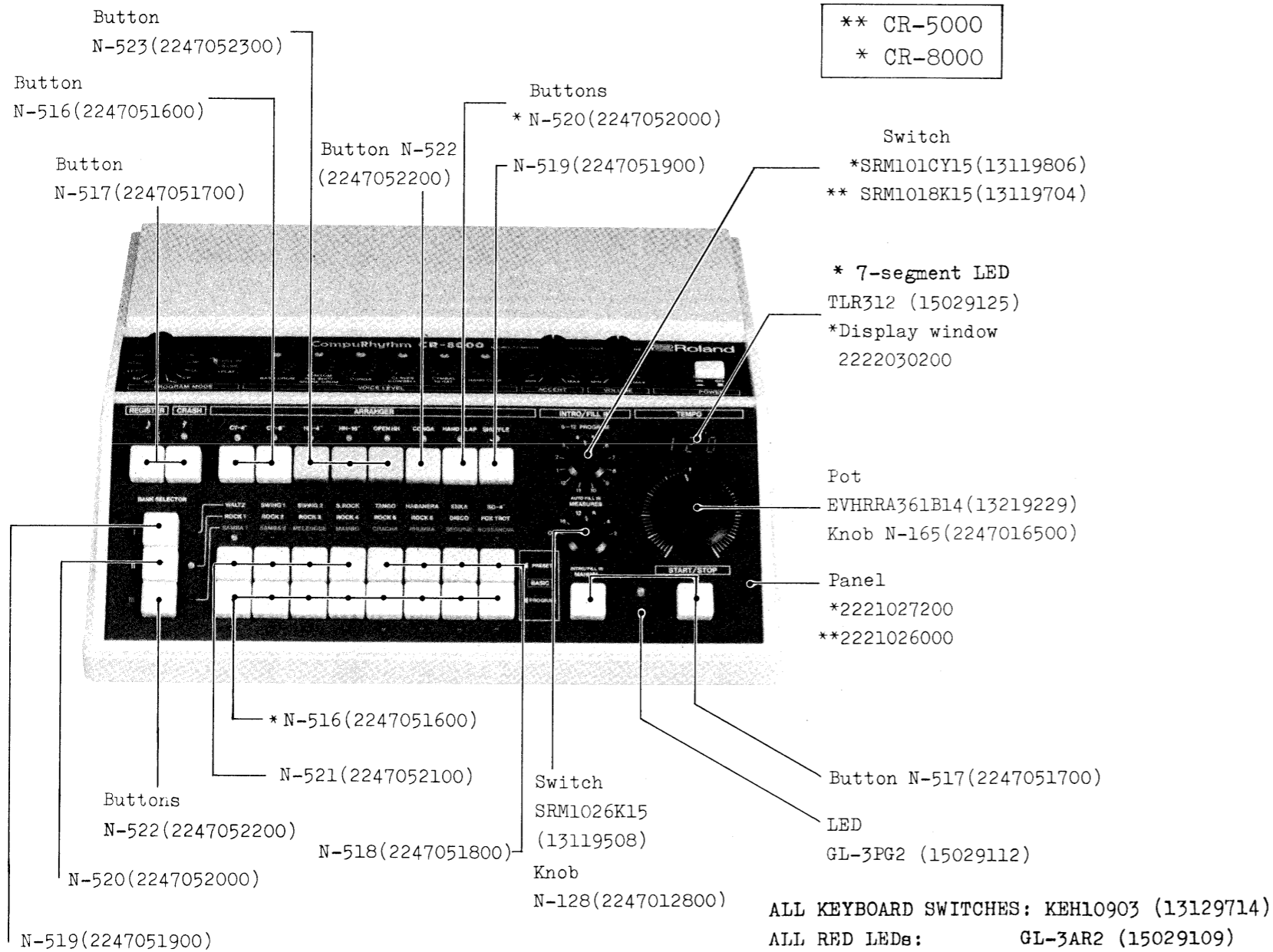
Second Printing (July 12, 1983 E2)

OUTPUT IMPEDANCE . . . . . Less than 6K $\Omega$  or less than 25K $\Omega$  (Serial No. CR5000 091100-, CR8000 090900-)  
 TRIGGER OUT . . . . . Level: +5 positive edge  
 Width: 44ms (typ) @ TEMPO min./12ms (typ) @ TEMPO max.  
 OUTPUT (max.) . . . . . 4V p-p @ VOICE LEVEL max./VOLUME max./ACCENT min. (16V p-p @ ACCENT max.)  
 (into 100K $\Omega$ ) 2.5V p-p @ VOICE LEVEL mid./VOLUME mid./ACCENT mid.  
 (CR8000)  
 SYNC IN . . . . . +15V (max.)  
 SYNC OUT . . . . . +15V (Tempo clock - 6.7ms-71ms)  
 POWER CONSUMPTION . . . . . CR5000: 10W, CR8000: 12W  
 DIMENSIONS . . . . . 331(W) x 278(D) x 108(H)mm  
 WEIGHT . . . . . 3.7kg  
 NOISE . . . . . 0.3mV rms (-68dB) (0dB = 0.775V)  
 (load 100k $\Omega$ ) (DIN 45405 wtd)



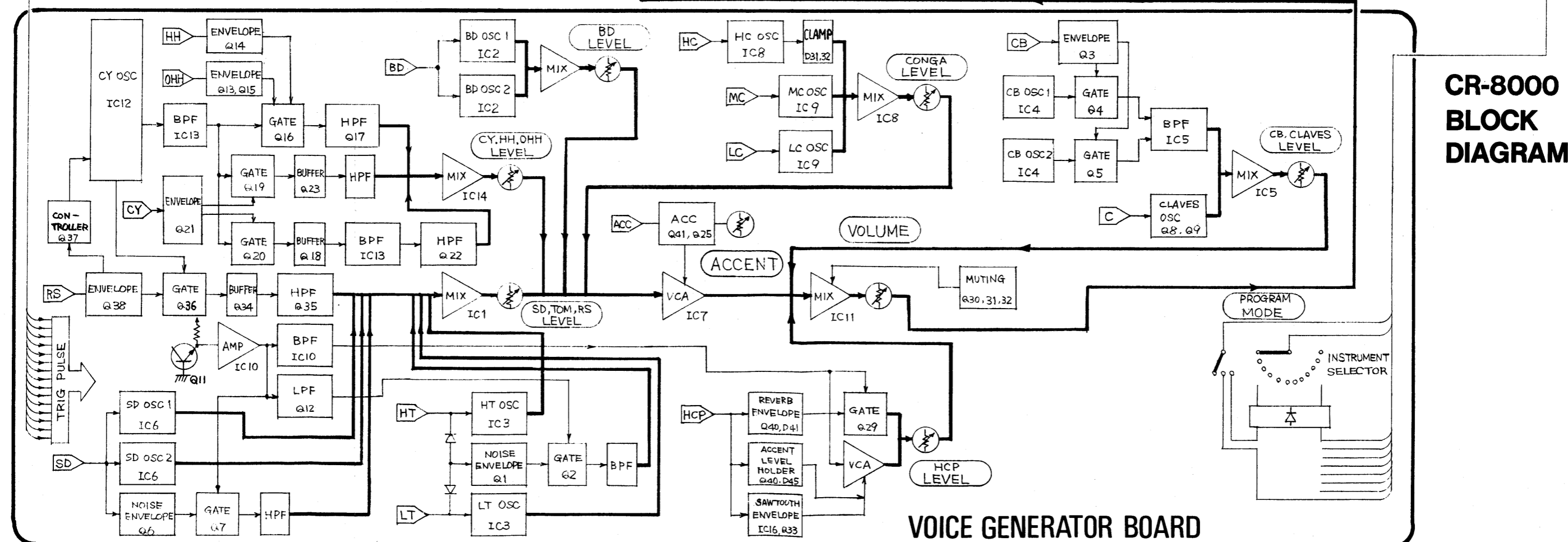
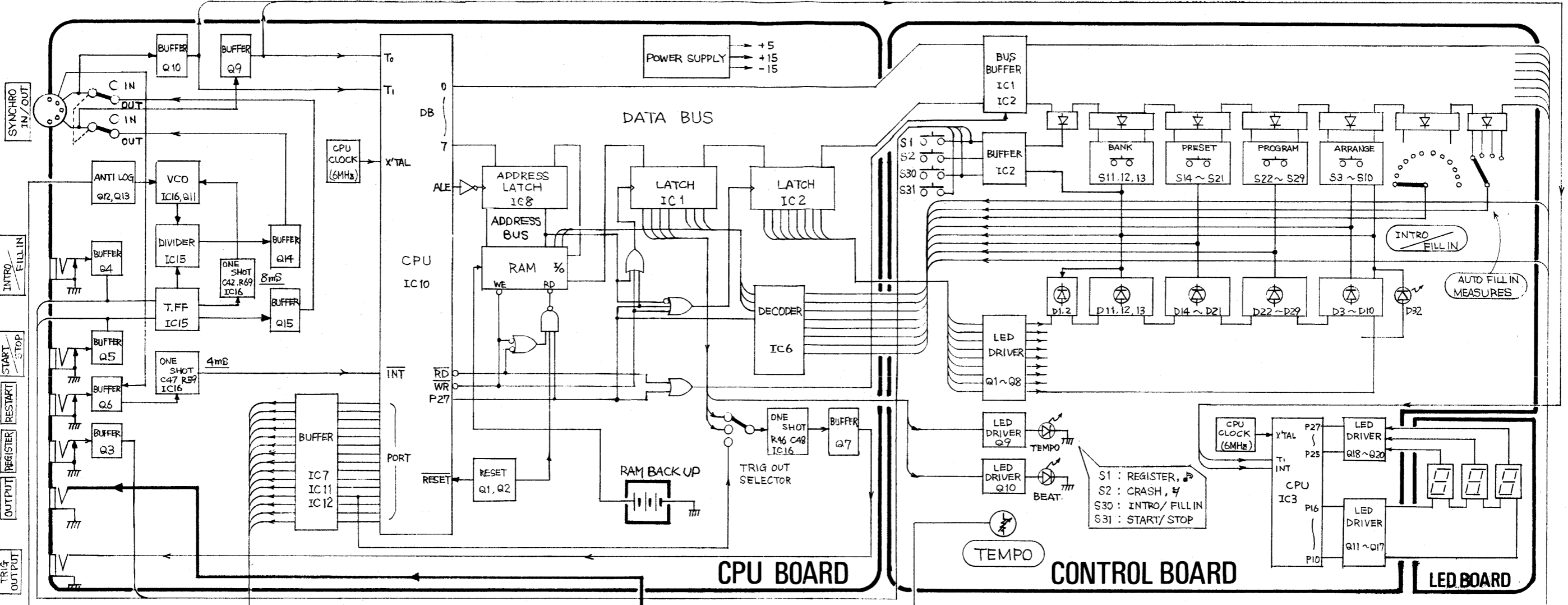
### DISASSEMBLY

Remove ten (10) screws indicated below.

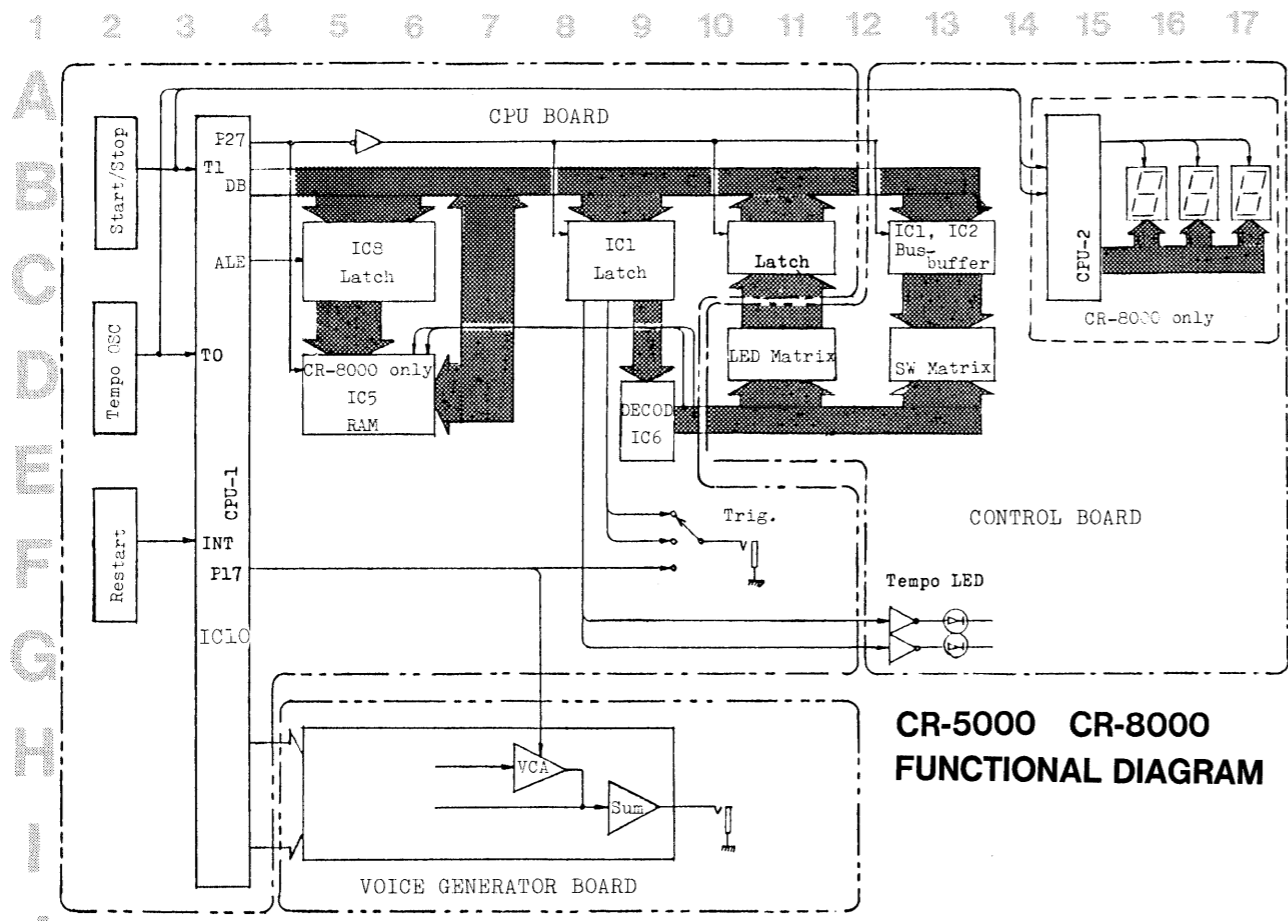


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V



CR-8000  
BLOCK  
DIAGRAM



CR-5000 CR-8000  
FUNCTIONAL DIAGRAM

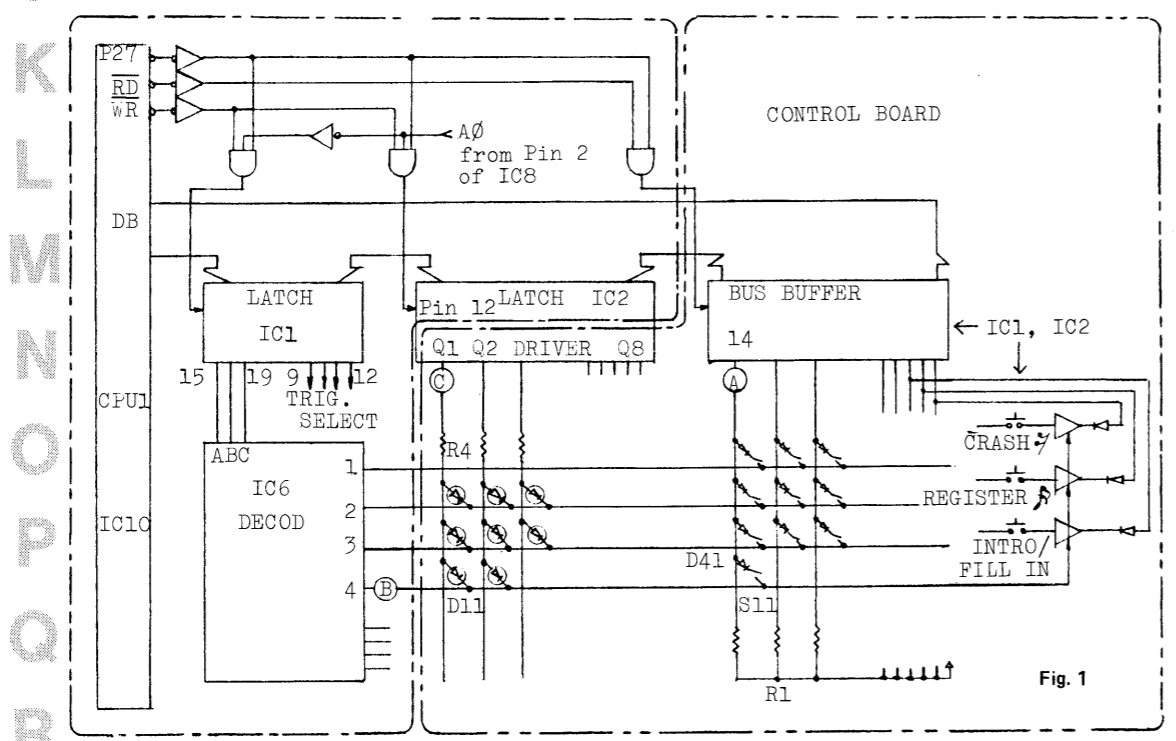
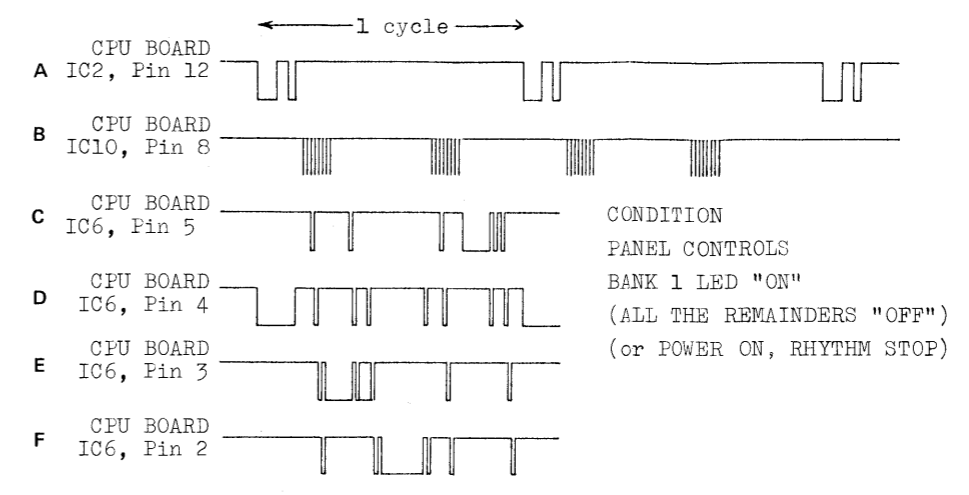
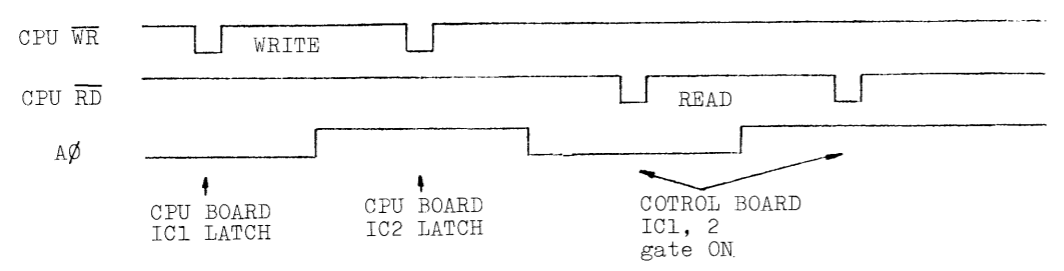


Fig. 1



CONDITION  
PANEL CONTROLS  
BANK 1 LED "ON"  
(ALL THE REMAINDERS "OFF")  
(or POWER ON, RHYTHM STOP)

Fig. 2

CIRCUIT DESCRIPTION

SWITCH SCANNING

CPU holds one of switch matrix rows low through LATCH IC1 and DECODER IC6. Exp. When S11 closes while pin 4 of IC6 (B in Fig. 1) is held low, pin 14 of BUFFER IC1 (A in Fig. 1) which is pulled up via R1, becomes low. This low is read by CPU through data bus. CPU continues this sequence for the remaining 7 matrix rows (B, Fig.2). Once rhythm starts, time interval between switch scanning varies to Tempo Clock rate.

LED DINAMIC SCANNING

To light LED that is on, CPU selects matrix row and column where the LED is connected diagonally. In the above example D11 has been on, CPU fires LED driver Q1 through LATCH IC2 in sympathy with low at B in Fig. 1 (A and D in Fig. 2.) Lengths of lows and intervals between lows in Fig. 2 also vary greatly with controls setting and rhythm tempo.

VOICE TRIGGER SIGNAL

CPU delivers trigger signals (negative going) to individual VOICE Generators. Trigger signal goes negative at the falling edge of tempo clock and stays low until the next falling edge of the tempo clock. That is, width of trigger signal is equal to period of one clock signal. The maximum trigger signal rate is  $\frac{24 \text{ clocks}}{4}$ .

EXT TRIGGER

Derived from LATCH IC1 on CPU board. They are also negative going and the pulse width is equal to that of tempo clock.

RESTART

CPU reads INT terminal (not in use for interrupt application) every 3ms and, when INT is high, resets internal counter to revert to onset of a measure. If monostable (1/6IC6, C47 and R59) output is high for a period shorter than 3ms or longer than 6ms, CPU may miss it or read twice at INT terminal; resultant is non return to the starting point of a two measure succession or quick double return.

A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V

**VOICE GENERATORS**

Most voice generators are designed based on a fashion similar to those detailed in the circuit description on the TR-808 Service Notes which is expected to be referenced to as necessary. Exceptions are Cymbal and Rim Shot. Below brief comments on individual voices.

**BD**

The circuit consists of two bridged-T networks.

**SD**

Also has two bridged-T filters for drum sound, in addition, noise generator for snare sound.

**LT. HT:**

Bridged-T networks in these stage include two diodes in their RC constant loop. The diode changes conducting rate in proportion to sound amplitude passing through the network, changing filter characteristic, thus shifts filter response curve (frequency) along sound contour. Pink noise is combined with this output to simulate reverbration.

**LC. MC. HC**

Also based on Bridged-T. HC output is clamped on D31 and D32 to have multiple harmonics to emphasis highs.

**HH. OHH. CY**

The combined square waves from Shmitt triggers IC2 are gated at choppers with the contour shaped by respective envelop generator outputs.

**RS**

Among six Schmitt triggers, two are used which are reset by an RS trig fed through Q37. The first rising edge of two outputs are synchronized to each other to eliminate unsavory sound at the very first of RS note.

**CB**

Two oscillator outputs of different frequency are summed at BPF after gated at choppers.

**HCP**

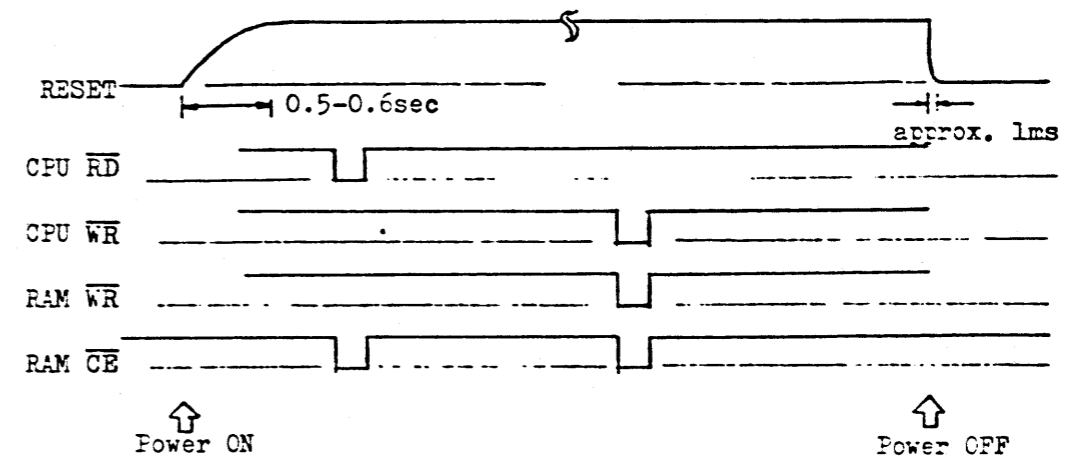
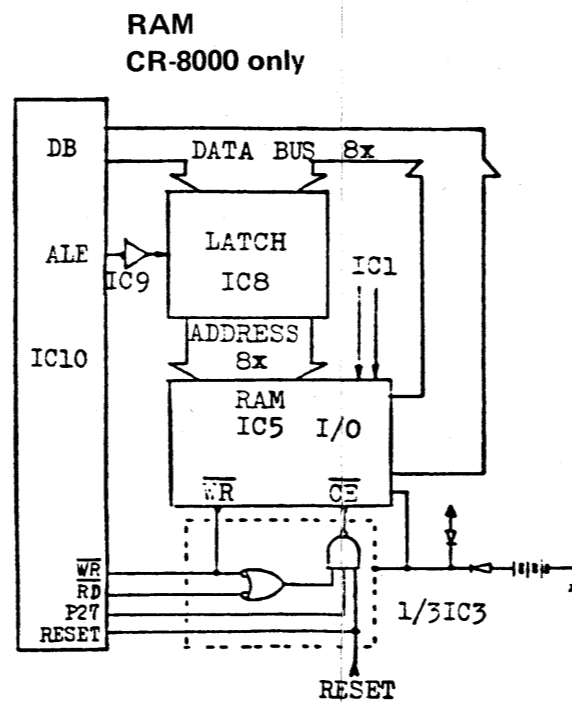
HCP sound is accomplished by modulating white noise with sawtooth waves derived from IC6.

**ACCENT**

Sounds passing through VCA IC7 are accentuated simaltenously when an accent pulse is applied to Q41 with its amplitude determined by VR8 setting.

**C (CLAVES)**

The circuit is designed based on conventional R-C phase oscillator.



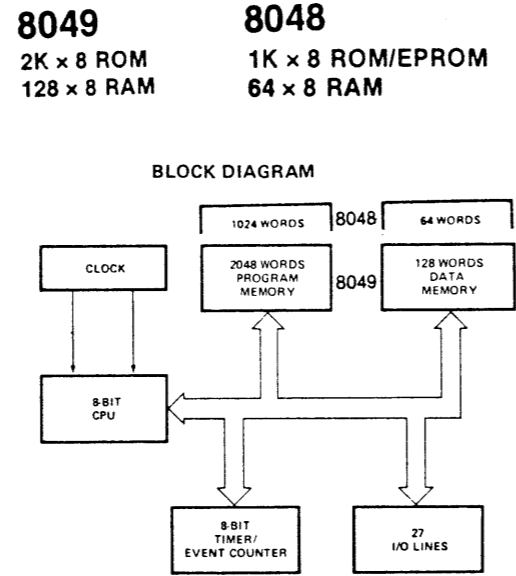
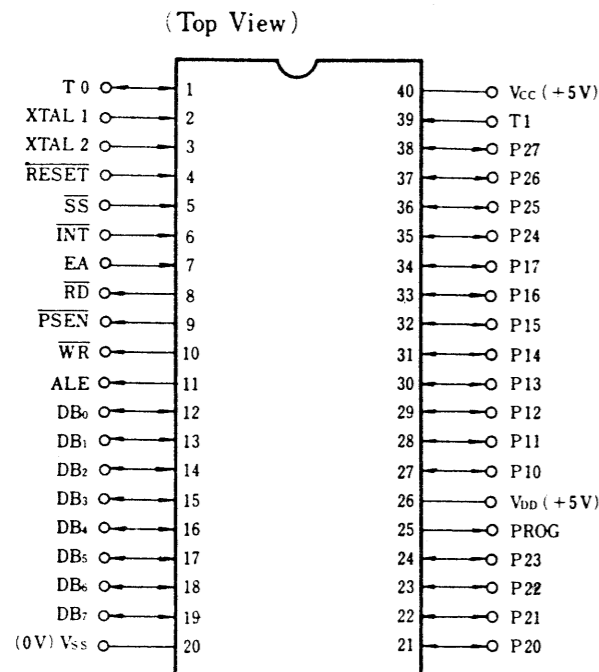
**NOTES:**

- P27 - high during RAM accessing
- CE - high during power off

Storage for programmed rhythm patterns are provided for the CR-8000. The memories are maintained by backup batteries (three 1.5V dry cells). The ten address bits are required to access to a memory location on 1024 words by 4 bit RAM uPD444; 8 bits are latched into IC8 by ALE and 2 bits into IC1 (also used for switch scanning).

μPD8049C/μPD8048C

SINGLE COMPONENT 8-BIT MICROCOMPUTER



μPD8049C

PIN NAME	PIN NO.	FUNCTION
T0	1	TEMPO CLOCK IN
T1	39	START/STOP SIGNAL IN
INT	6	RESTART SIGNAL IN
DATA BUS	12-19	SWITCH SCANNING OUT/IN LEDs LIGHT OUT TEMPO LED, TRIG OUT MEMORY READ/WRITE (CR-8000 only)
PORT 1		TRIGGER OUT FOR VOICE GENERATOR
P10	27	CYMBAL
P11	28	HI TOM
P12	29	OPEN HI-HAT
P13	30	LOW TOM
P14	31	HI-HAT
P15	32	SNARE DRUM
P16	33	BASS DRUM
P17	34	ACCENT
PORT 2		TRIGGER OUT FOR VOICE GENERATOR
P20	21	HI CONGA
P21	22	MIDDLE CONGA
P22	23	LOW CONGA
P23	24	COWBELL
P24	35	CLAVES
P25	36	RIM SHOT
P26	37	HAND CLAP
P27	38	I/O SELECT (SWITCH, LED BLOCK or RAM BLOCK)

uPD8049C-159  
 uPD8049C-232 (improved version)

The following program bug is eliminated in the -232 version.

Condition SHUFFLE ON with alternate rhythm patterns selected.

INTRO/FILL IN is pushed after the termination of first measure pattern.

When INTRO/FILL IN part ends, CPU delivers rhythm pattern data for the first measure but replaces the first step data only with the one for the second measure.

This is perceptible in RHUMBA, BEGUINE or BOSSANOVA.

μPD8048C CR-8000 only

PIN NAME	PIN NO.	FUNCTION
T0	1	NO APPLICATION (KEPT LOW)
T1	39	TEMPO CLOCK IN
INT	6	START/STOP SIGNAL IN
DATA BUS	12-19	KEPT HIGH for Internal program initialization KEPT LOW KEPT LOW NO CONNECTION
PORT 1		
P10	27	7-SEGMENT LED LIGHT SIGNAL OUTPUTS
P11	28	
P12	29	
P13	30	
P14	31	
P15	32	
P16	33	
P17	34	NO CONNECTION
PORT 2		
P20-P23	21-24	NO CONNECTION
P24	35	(NOT IN USE)
P25	36	7-SEGMENT LED
P26	37	CONTROL SIGNAL
P27	38	OUTPUT

TEMPO DISPLAY (CR-8000 only)

uPD8048C IC3 on Control Brd counts Tempo Clocks derived from Q9 on CPU Brd whenever power is being fed to the CR-8000.

Since 24 tempo clocks are made equal to one J, actual tempo displayed is

$$\frac{\text{clocks per minute}}{24}$$

CPU performs an equivalent eq. in a short period and drives Q18-Q20 on Control Brd in synchronous with drive signals for 7 segments of display LEDs.

Upon rhythm running INT of CPU IC3 goes and stays negative with which CPU's internal count gate is disabled, then re-started at the first falling edge of the next tempo clock. This count break allows CPU to skip transitional tempo clock that is reset by a start signal.

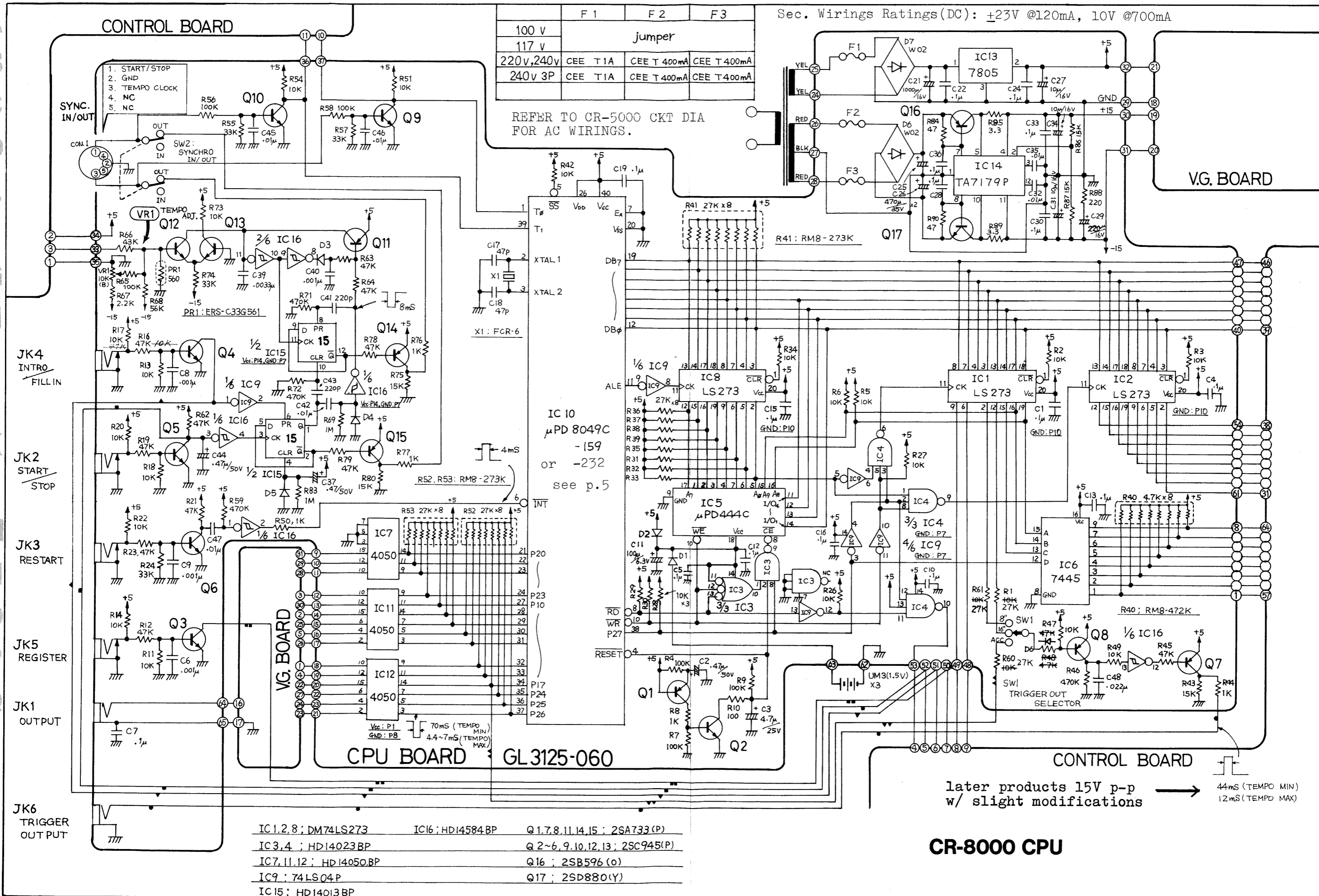
If INT remains high after rhythm running, tempo display varies temporarily.

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42

Sec. Wirings Ratings(DC): ±23V @120mA, 10V @700mA

	F 1	F 2	F 3
100 v			
117 v	jumper		
220v,240v	CEE T 1A	CEE T 400mA	CEE T 400mA
240v 3P	CEE T 1A	CEE T 400mA	CEE T 400mA

REFER TO CR-5000 CKT DIA FOR AC WIRINGS.



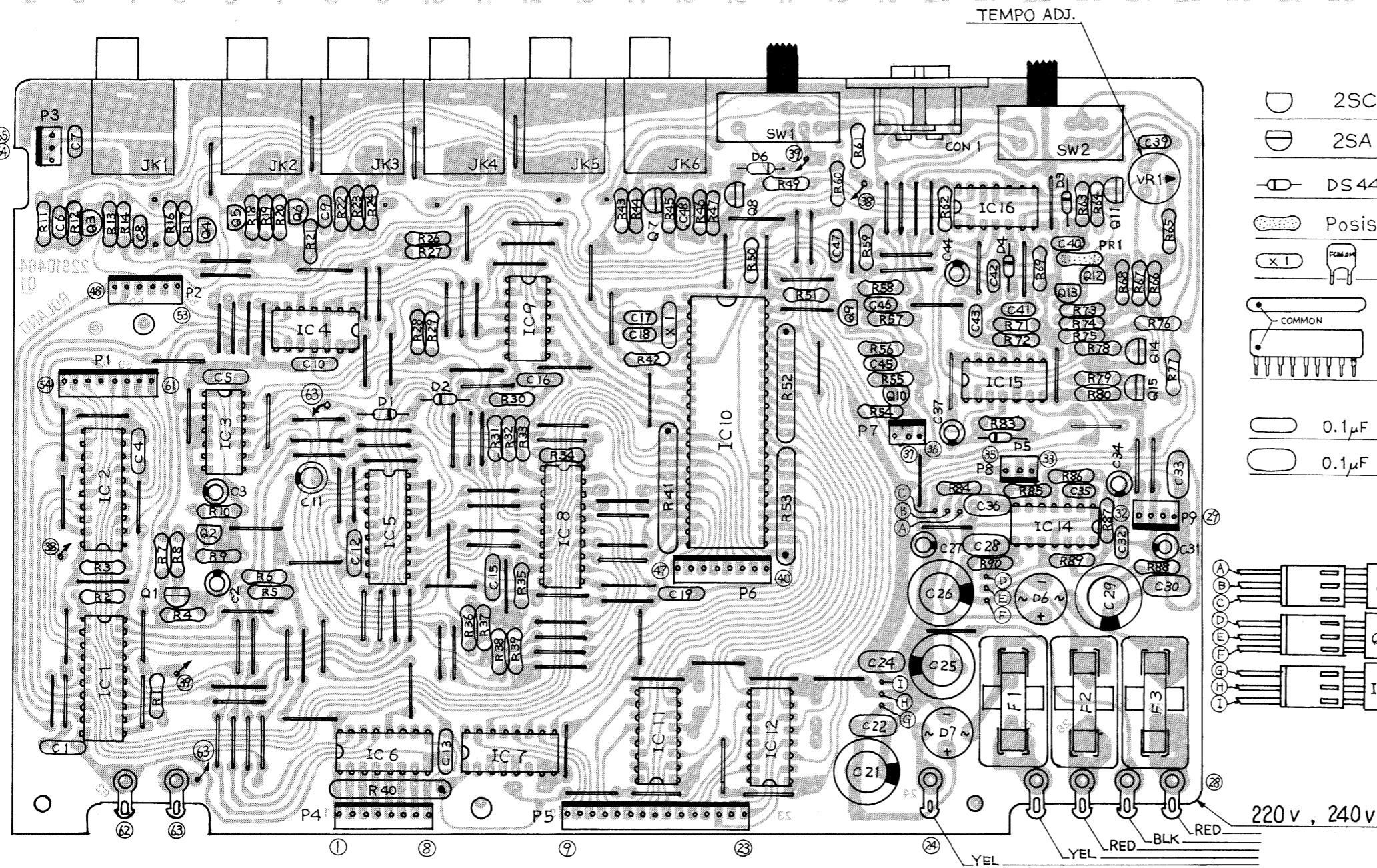
- IC 1,2,8; DM74LS273
- IC 3,4; HD14023BP
- IC 7,11,12; HD14050BP
- IC 9; 74LS04P
- IC 15; HD14013BP
- IC 16; HD14584BP
- Q 1,7,8,11,14,15; 2SA733(P)
- Q 2~6,9,10,12,13; 2SC945(P)
- Q 16; 2SB596(o)
- Q 17; 2SD880(Y)

CR-8000 CPU

later products 15V p-p w/ slight modifications → 44ms (TEMPO MIN) 12ms (TEMPO MAX)

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V



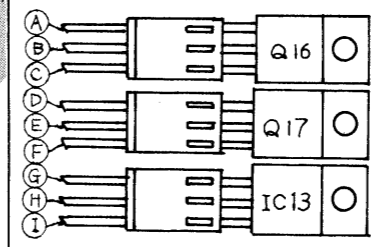
- 2SC 945 P
- 2SA 733 P
- DS 442 or 1S2473
- Posistor ERS-C33G561
- Ceramic Resonator
- Resistor Array  
R40, R41 R52 R53
- 0.1µF Ceramic
- 0.1µF Mylar

**CR-8000  
CPU BOARD  
GL3125-060  
(731250600)  
(pcb 2291046401)**

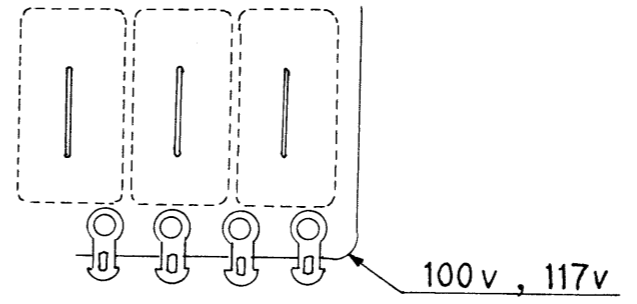
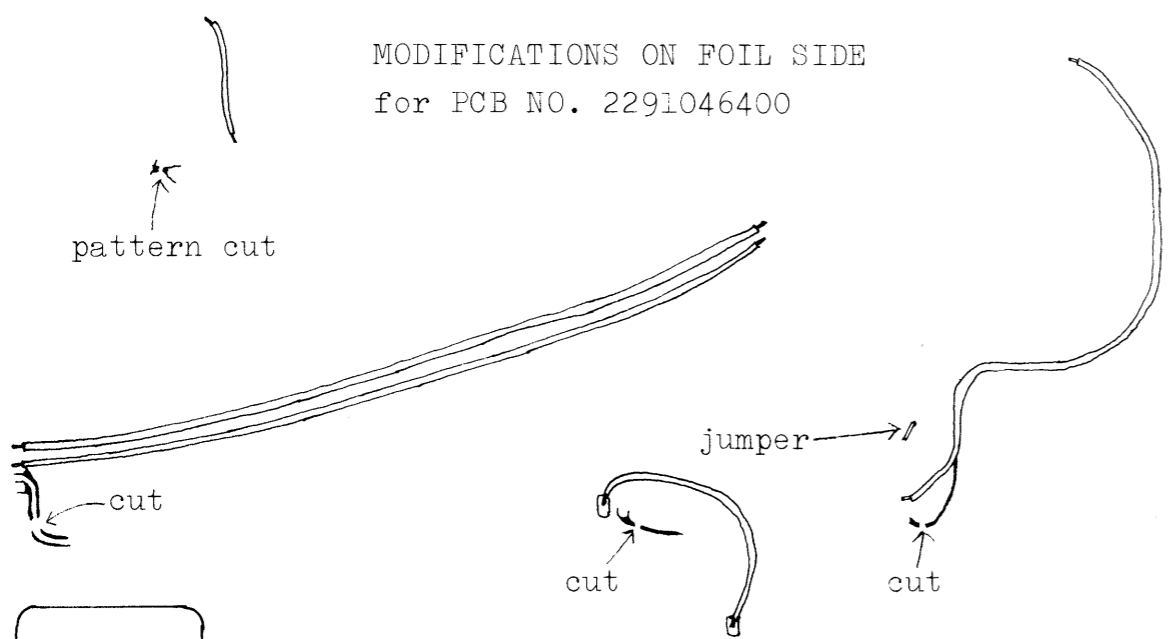
CHANGES IN COMPONENTS

Ensure trigger outputs at IC1 when low VOH

- LS273 is used.
- R47 47k to 10k
- R48 47k to D6
- R1 10k to 27k
- R61 10k to 27k
- R60 10k to 27k



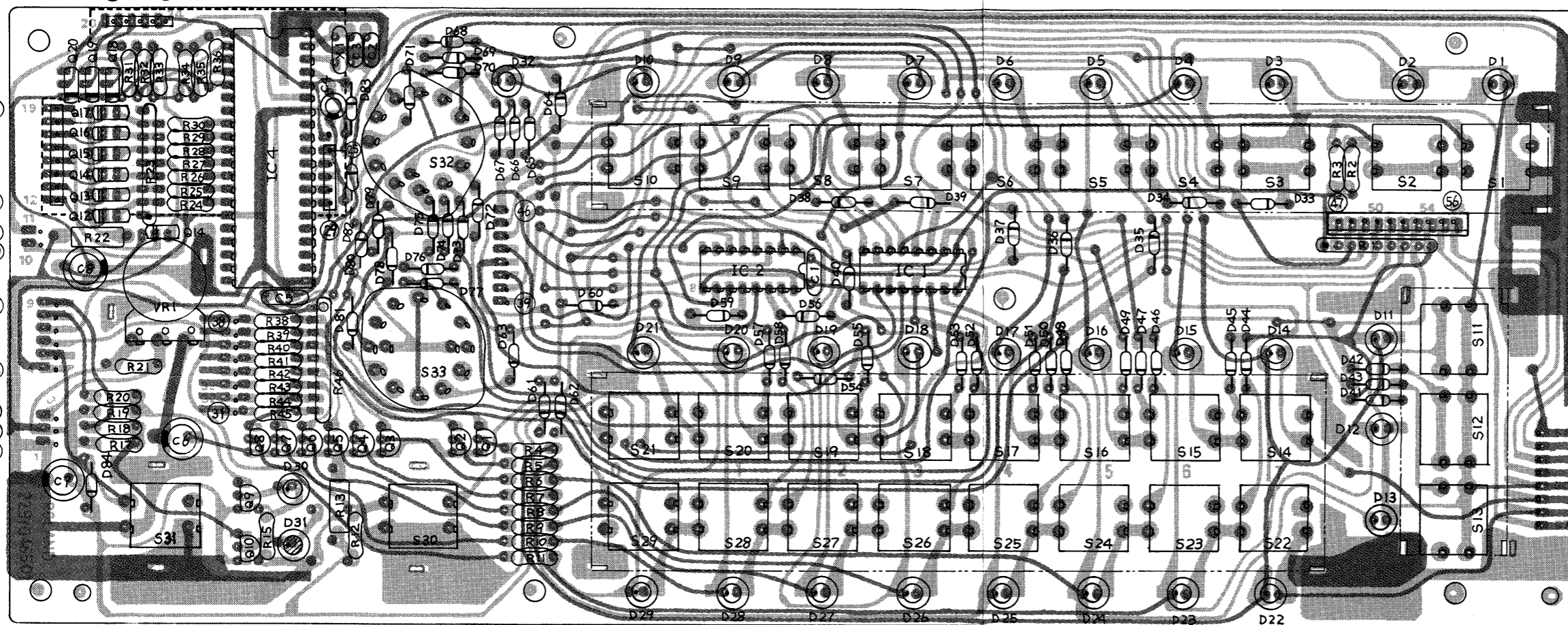
MODIFICATIONS ON FOIL SIDE  
for PCB NO. 2291046400



CONTROL BOARD GL3125-090 (7312509008) (pcb 2291046501)

Serial Number 142650 and higher

(Viewed from the rear)

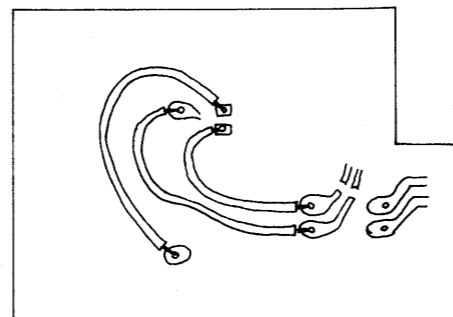
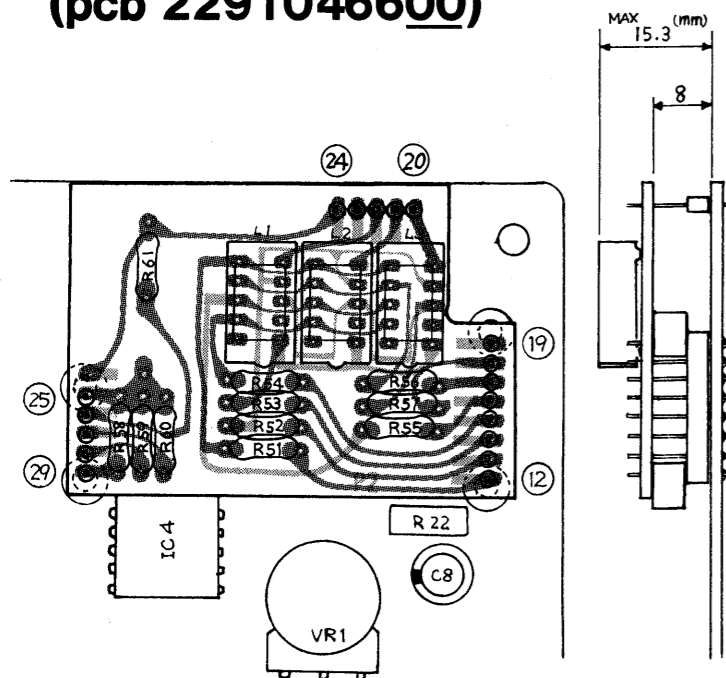
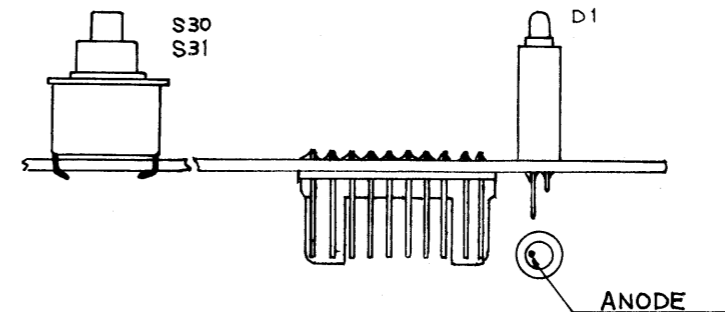


Refer to p.16 for pcb 2291046500: surface mounting jumper wire.

CR-8000

LED BOARD (7312511001) (pcb 2291046600)

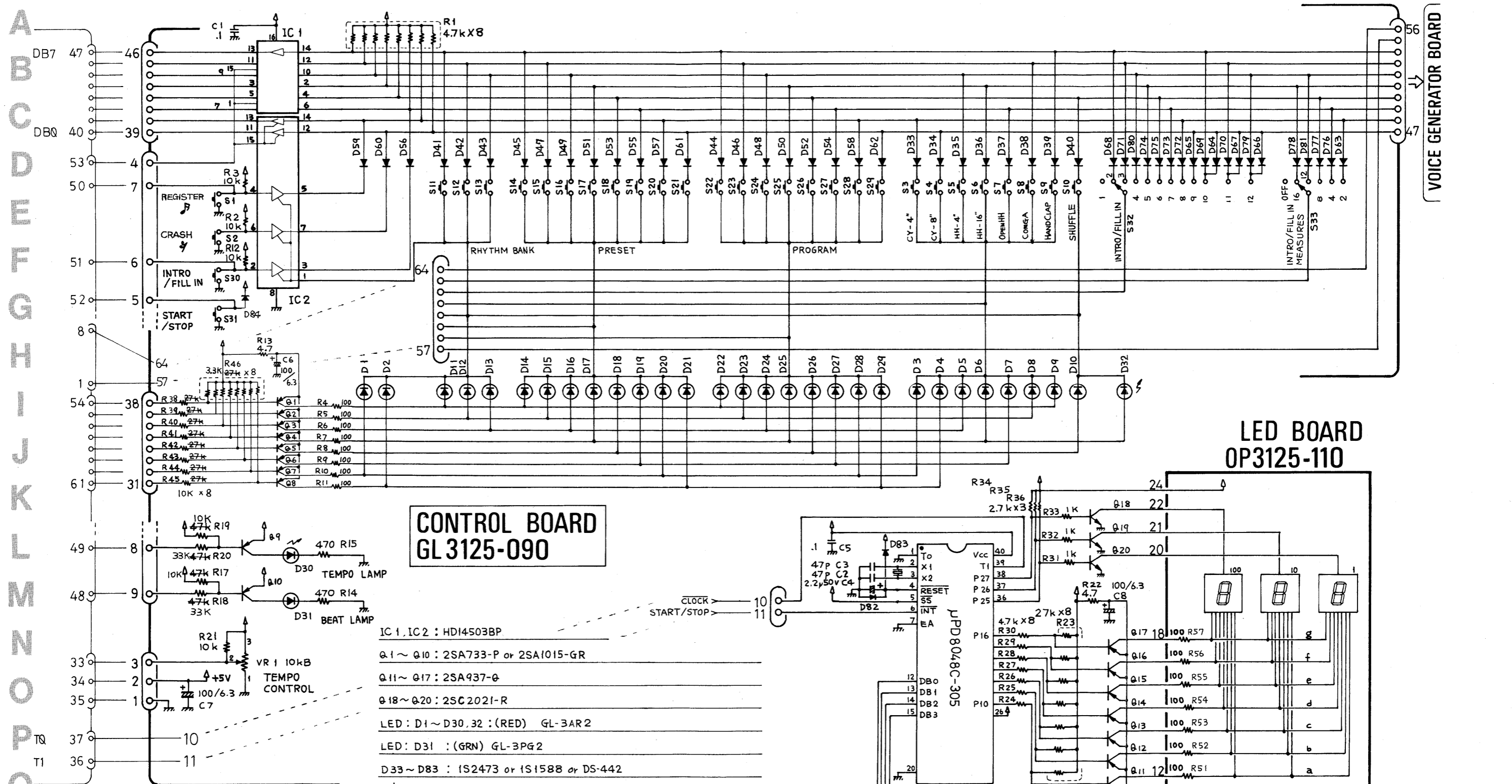
LED BOARD on early products pcb 2291046600 without underscore Pattern cuts, Jumpers



- D- : DS442 or 1S1588, 1S2473
- : 2SA733P or 2SA1015GR
- : 2SA937Q
- ▭ : 2SC2021R
- X1 : CERAMIC RESONATOR (6.0MHz) FCR-6
- ⊙ : LED GL-3PR2 (RED)
- ⊗ : LED GL-3PG2 (GRN)



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40



**CONTROL BOARD  
GL 3125-090**

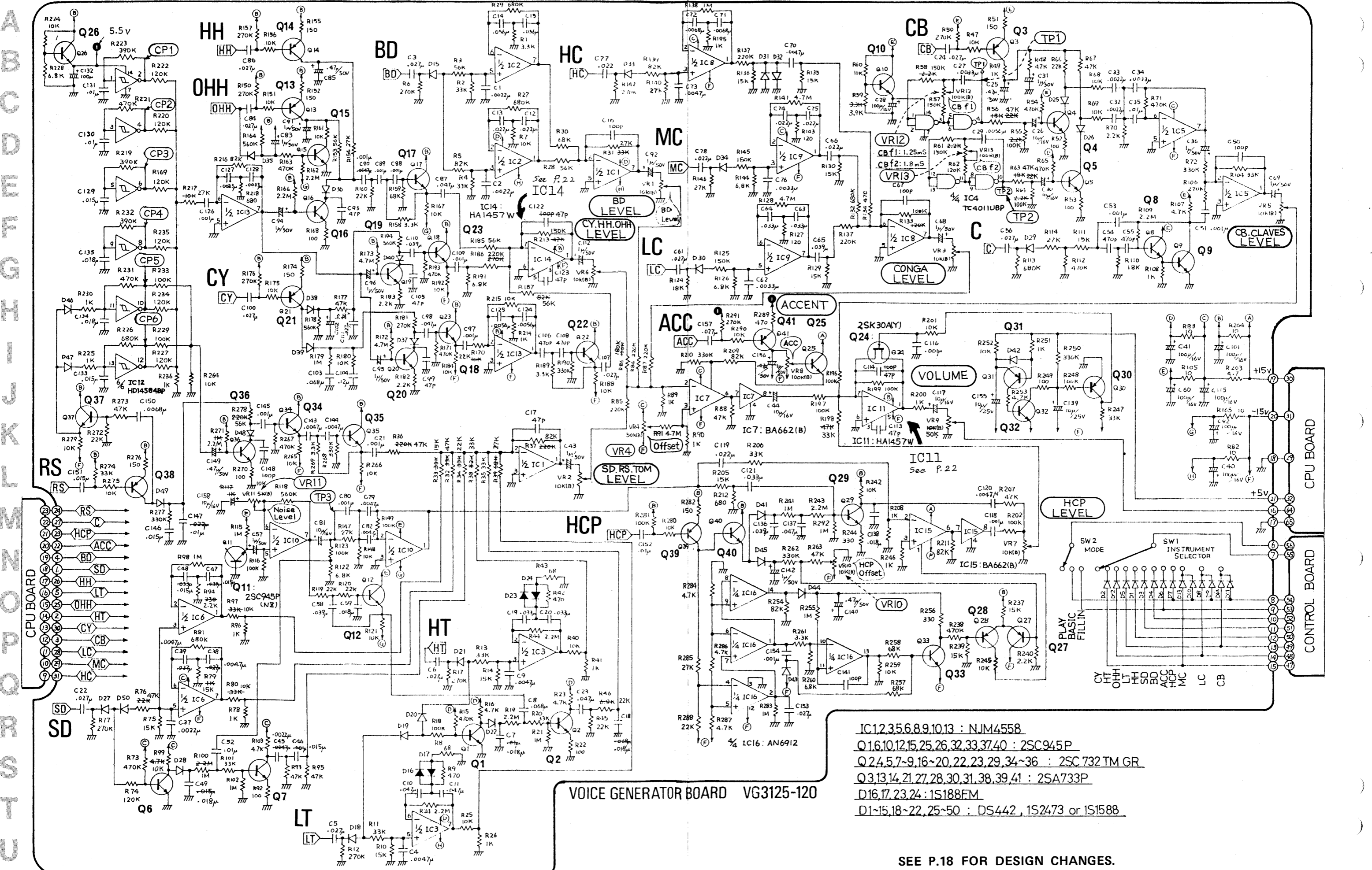
- IC 1, IC 2 : HDI4503BP
- Q1 ~ Q10 : 2SA733-P or 2SA1015-GR
- Q11 ~ Q17 : 2SA937-θ
- Q18 ~ Q20 : 2SC2021-R
- LED : D1 ~ D30, 32 : (RED) GL-3AR2
- LED : D31 : (GRN) GL-3PG2
- D33 ~ D83 : 1S2473 or 1S1588 or DS-442
- CERAMIC RESONATOR : (6.0MHz) FCR-6/TDK

**CR-8000 CONTROL**

CHANGES IN RESISTANCE With Serial Number 090900 and up  
 The changes eliminates possible dim lighting of LEDs due to insufficient H level output at IC1 or IC2 on CPU board:  
 R38-R45: 27k to 10k      R17, R19: 47k to 10k      R18, R20: 47k to 33k  
 Resistor Array R46: 27k to 3.3k

A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42

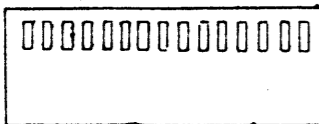


- IC 1,2,3,5,6,8,9,10,13 : NJM4558
- Q 1,6,10,12,15,25,26,32,33,37,40 : 2SC945P
- Q 2,4,5,7-9,16~20,22,23,29,34~36 : 2SC 732 TM GR
- Q 3,13,14,21,27,28,30,31,38,39,41 : 2SA733P
- D 16,17,23,24 : 1S188FM
- D 1~15,18~22,25~50 : DS442, 1S2473 or 1S1588

SEE P.18 FOR DESIGN CHANGES.

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V



early PCB: R117 1k $\Omega$   
S/N 101300--: C158

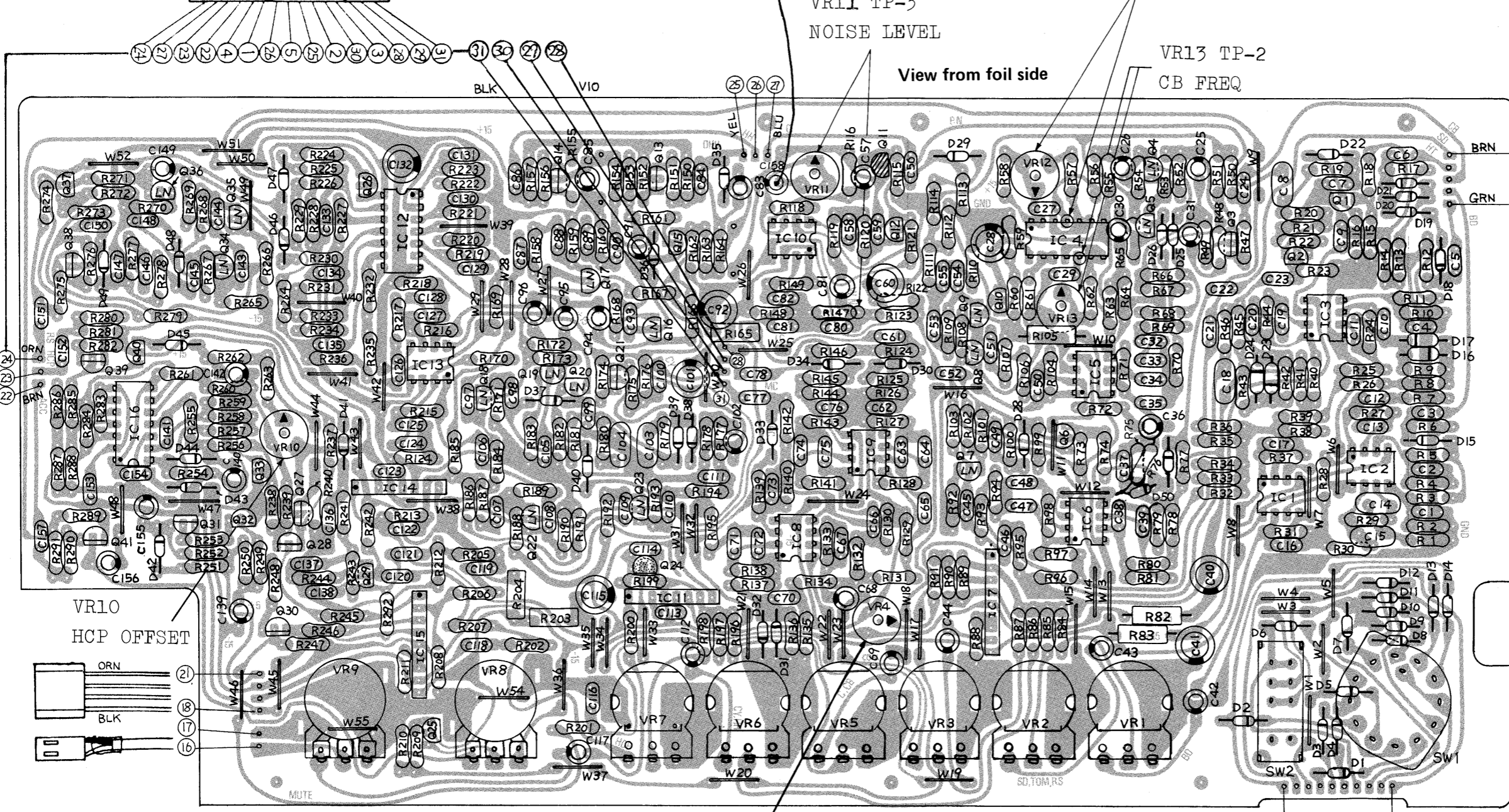
VR12 TP-1  
CB FREQ

VR11 TP-3  
NOISE LEVEL

VR13 TP-2  
CB FREQ

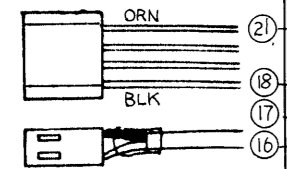
View from foil side

- 2SC945-P
- 2SC732TM-GR
- 2SA733-P
- 2SC945-P(NZ)
- 2SK30A-Y
- DS442, 1S2473 or 1S1588
- 1S188FM



**CR-8000  
VOICING BOARD  
VG3125-120  
(7312512007)  
(pcb 2291046302)**

VR10  
HCP OFFSET



VR9

VR8

VR7

VR6

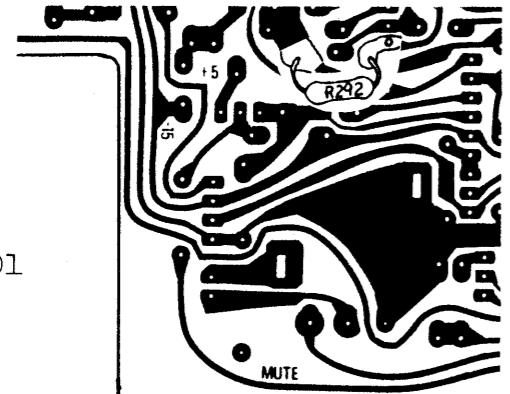
VR5

VR3

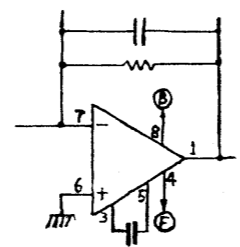
VR2

VR1

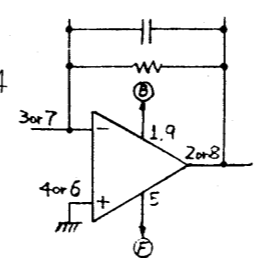
VR4 OFFSET



surface  
mounting  
on PCB  
2291046301



IC11, IC14



HA1457W (8 pins) or NJM4558S (9 pins) (See p. 22 for detail.)

CHANGES IN COMPONENTS  
with S/N 090900  
VR9 from 10k to 50k  
Eliminates whizz sound  
upon power off.

with S/N 101300  
R198(HCP) 47k to 33k

with S/N 111700  
R55,56,58,61,63,64  
resistances are increased  
to limit currents into  
IC4. This modification is  
mandatory when replacing  
defective IC4.

ALSO SEE CR-5000 VG BRD  
LAYOUT FOR OTHER MODIFI-  
CATIONS.

### ADJUSTMENTS

#### CPU BOARD

RAM BACK UP BATTERIES (CR-8000 only)  
 Power switch must be turned OFF.  
 Connect 100 ohms across pins 18 (Vcc) and 9 (GND) of RAM IC5 or shunt meter (scope or voltmeter) inputs with 100 ohms. Confirm approx. 4V at pin 18.

#### TEMPO CLOCK

Allow at least 10 minutes for circuit thermal stabilization.

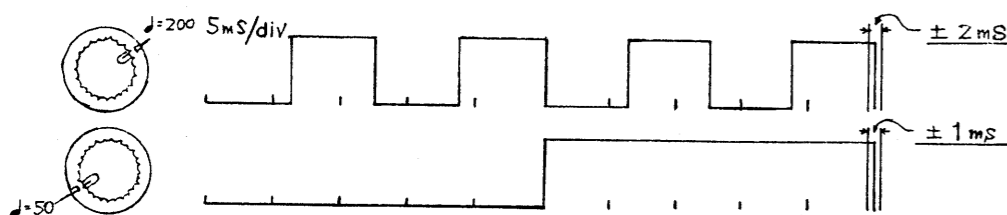
#### CR-5000

Connect scope to pin 1 of CPU (TP-1). Set scope time base to 5ms/div. With TEMPO set at 200 adjust VR1 for 12.5ms/cycle (50ms/4 cycles). Reset TEMPO to 50 and confirm that 1 cycle is 50m±lms. If exceeds this limit, readjust VR1 for lms at the sacrifice of ±2ms error at TEMPO 200.

#### CR-8000

Turning TEMPO across its travel, confirm TEMPO DISPLAY; factory set ranges from 33±2 to 375±5%. Adjust VR1 as required.

NOTE: TEMPO =  $\frac{2500}{\text{period of one tempo clock cycle (ms)}}$



#### VOICE BOARD

#### NOISE

Connect scope (1V/div, time base relatively slow) to TP-3. Adjust VR11 for 2V p-p when measured at rather dense peaks.

#### CB

Connect scope to TP-1. Adjust VR12 for 1.25ms/cycle. Connect scope to TP-2. Adjust VR13 for 1.8ms/cycle.

#### CY

See table right. Probing CP1-CP6 of oscillators IC6, confirm frequency ratios between adjacent two; they should be in 1.1-1.4 steps. Note that two oscillators generating on too close frequency will sound beating cymbal which can be eliminated by tailoring R and C listing on the table.

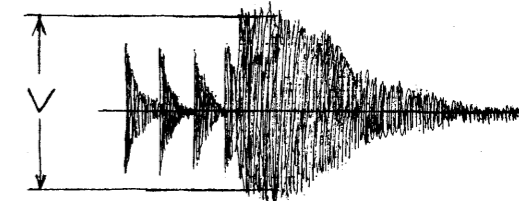
#### OFFSET

Controls set up - All VOICE LEVELs: FCCW; VOLUME, ACCENT: MAX; RYTHM: DISCO Start the rythm. Monitoring through OUTPUT jack (scope or amp), adjust VR4 for minimum thump.

#### HCP (CR-8000 only)

Controls set up - HCP VOICE LEVEL: FCW; VOLUME: MAX; ARRANGER: HAND CLAP Connect scope V IN to OUTPUT jack and H (EXT) to HCP trig terminal 23. Adjust VR10 for the below:

Serial number up to 101299 1V p-p  
 Serial number 101300 and up 2V p-p



CHECK POINT	FREQUENCY (mS)(Hz)			AMPLITUDE (V <sub>p-p</sub> )			DECAY TIME (mS)			VOICE LEVEL CONTROL AT HOT TERMINAL			OUTPUT JACK				
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	AMPLITUDE (V <sub>p-p</sub> )				
BD	H IC2 PIN1	13.2 (76)	11.4 (88)	9.7 (103)	6.8	7.6	8.4	30	40	50	6.7	8.0	9.6	77	96	115	1.2
	L IC2 PIN7	20.2 (50)	17.5 (57)	15.0 (67)	11.9	13.2	14.5	90	100	110							
SD	H IC6 PIN1	3.5 (286)	3.0 (333)	2.5 (400)	4.7	5.6	6.5	8	10	12	10.8	13.0	15.6	58	72	86	1.7
	L IC6 PIN7	5.1 (196)	4.4 (227)	3.8 (266)	16.8	20.0	23.2	28	34	40							
LT	IC3 PIN7	10.9 (91.7)	9.4 (106)	8.0 (124)	24	27	28				7.0	8.8	10.6	160	200	240	1.3
HT	IC3 PIN1	7.6 (132)	6.6 (152)	5.6 (177)	24	27	28				4.6	6.0	7.4	120	150	180	1.0
LC	IC9 PIN7	5.8 (172)	5.0 (200)	4.3 (234)	24	27	28				6.4	8.0	9.6	136	170	200	1.3
MC	IC9 PIN1	3.9 (256)	3.4 (294)	2.9 (343)	24	27	28				2.2	2.8	3.4	80	100	120	0.4
HC	IC8 PIN1	1.67 (599)	1.45 (690)	1.24 (807)	24	27	28				3.4	4.3	5.1	12	15	18	0.6
CB	TP1,VR12 TP2,VR13		1.25 (800) 1.80 (555)								1.1	1.3	1.6	29	36	43	1.3
C	Q9 COLLECTOR	0.49 (2.01K)	0.43 (2.33K)	0.37 (2.72K)							1.3	1.6	1.9	11	14	17	1.5
HCP	VR10										0.4	0.6	0.8	72	90	108	2.0

CHECK POINT	R (KΩ)	C (μF)	FREQUENCY (mS)(Hz)		
			MIN	TYP	MAX
CP 1	R233	C131			
	390	0.01	1.58 (631)	1.26 (794)	
CP 2	R221	C130			
	470	0.01		1.54 (649)	
CP 3	R219	C129			
	390	0.015		1.91 (524)	
CP 4	R232	C135			
	390	0.018		2.25 (444)	
CP 5	R231	C134			
	470	0.018		2.72 (368)	
CP 6	R226	C133			
	680	0.015	4.20 (238)	3.53 (283)	

RS	18.4	23	27.6	24	30	36	2.6
CY	6.3	7.6	9.1	300	380	450	1.2
HH	5.8	7.0	8.4	59	74	89	1.1
OHH	5.8	7.0	8.4	240	300	360	1.1

CR-5000 S/N with 101400 -  
 CR-8000 S/N with 101300 -

Ref. set up  
 VOICE LEVEL, VOLUME: MAX  
 ACCENT : MIN  
 (@ MAX, add 12dB to each:  
 four times MIN.)

CHECK POINT	FREQUENCY (mS)(Hz)			AMPLITUDE (V <sub>p-p</sub> )			DECAY TIME (mS)			VOICE LEVEL CONTROL AT HOT TERMINAL			OUTPUT JACK				
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	AMPLITUDE (V <sub>p-p</sub> )				
BD	H IC2 PIN1	13.2 (76)	11.4 (88)	9.7 (103)	6.8	7.6	8.4	30	40	50	7.2	9.0	10.8	77	96	115	1.5
	L IC2 PIN7	20.2 (50)	17.5 (57)	15.0 (67)	11.9	13.2	14.5	90	100	110							
SD	H IC6 PIN1	4.4 (227)	3.8 (263)	3.2 (308)	24	27	28	54	64	74	9.6	12.0	14.4	58	72	86	1.7
	L IC6 PIN7	5.1 (196)	4.4 (227)	3.8 (266)				30	40	50							
LT	IC3 PIN7	10.9 (91.7)	9.4 (106)	8.0 (124)							7.2	9.0	10.8	160	200	240	1.5
HT	IC3 PIN1	7.6 (132)	6.6 (152)	5.6 (177)							5.6	7.0	8.4	120	150	180	1.0
LC	IC9 PIN7	5.8 (172)	5.0 (200)	4.3 (234)							6.4	8.0	9.6	136	170	200	1.3
MC	IC9 PIN1	3.9 (256)	3.4 (294)	2.9 (343)							2.4	3.0	3.6	80	100	120	0.5
HC	IC8 PIN1	1.67 (599)	1.45 (690)	1.24 (807)							3.4	4.3	5.1	12	15	18	0.6
CB	TP1,VR12 TP2,VR13		1.25 (800) 1.80 (555)								1.1	1.3	1.6	29	36	43	1.3
C	Q9 COLLECTOR	0.49 (2.01K)	0.43 (2.33K)	0.37 (2.72K)							1.3	1.6	1.9	11	14	17	1.5
HCP	VR10										0.4	0.6	0.8	72	90	108	1.0

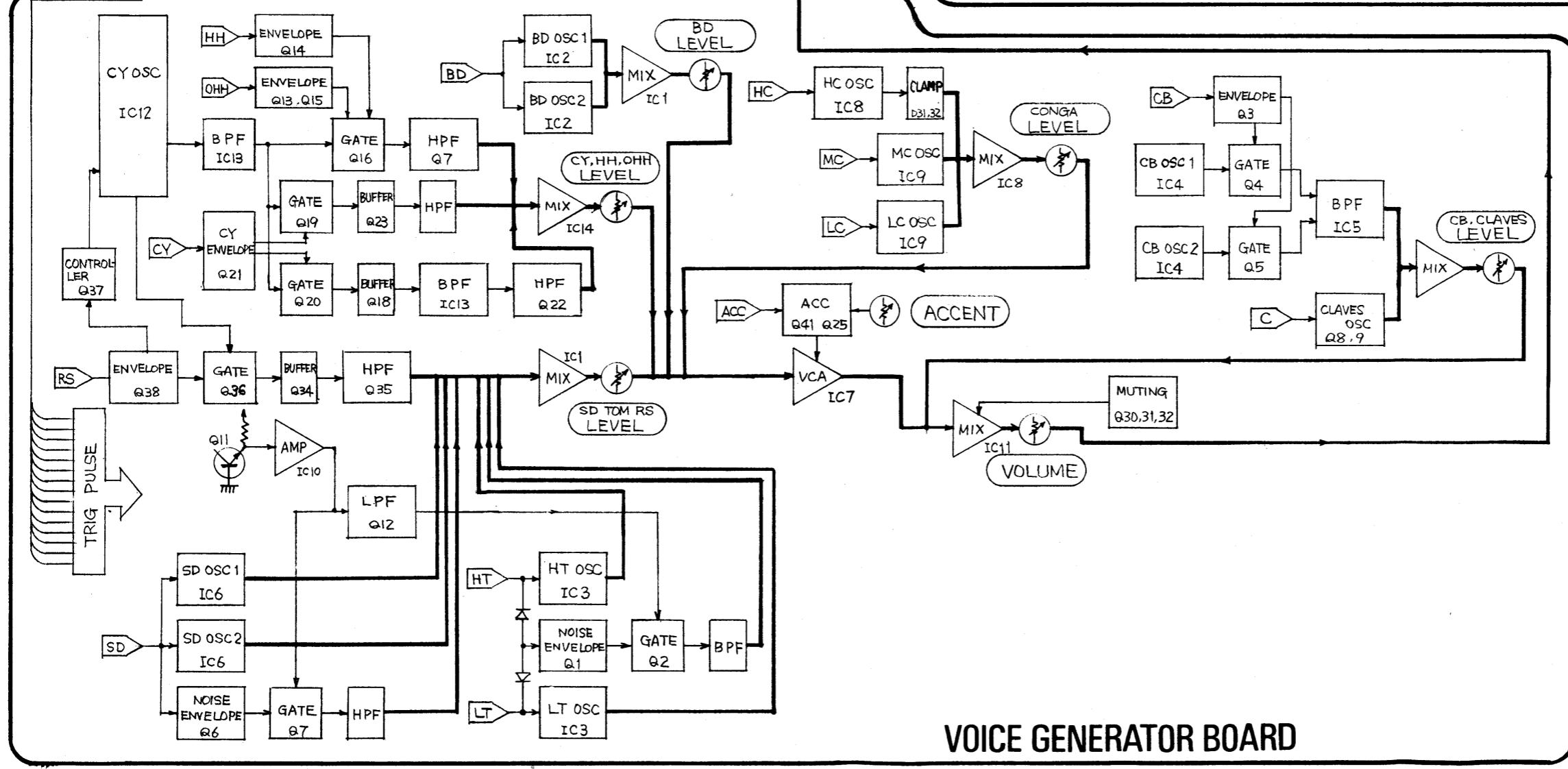
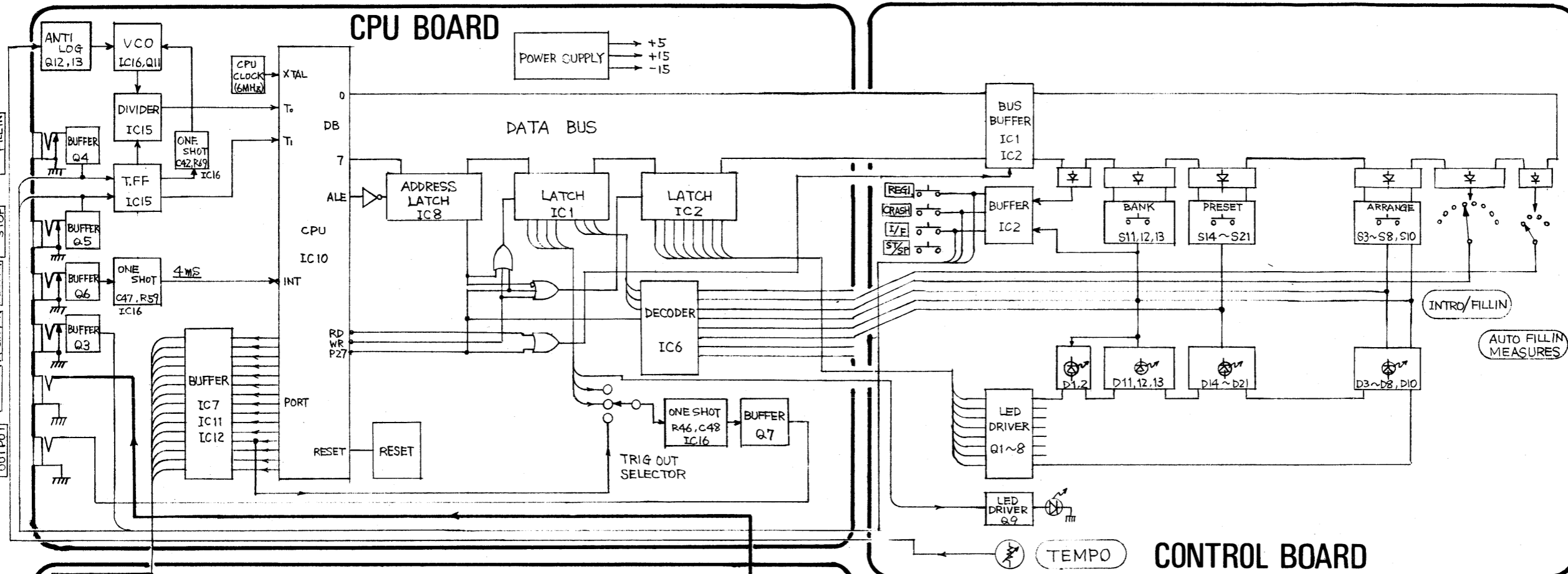
CR-5000 S/N up to 101399  
 CR-8000 S/N up to 101299

RS	10	13	16	24	30	36	1.5
CY	2.5	3.5	4.5	300	380	450	1.0
HH	3.0	4.0	5.0	59	74	89	1.0
OHH	3.0	4.0	5.0	240	300	360	1.0

See table above for RS, CY, HH and OHH frequencies.

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

A  
B  
C  
D  
E  
F  
G  
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I  
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K  
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O  
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V

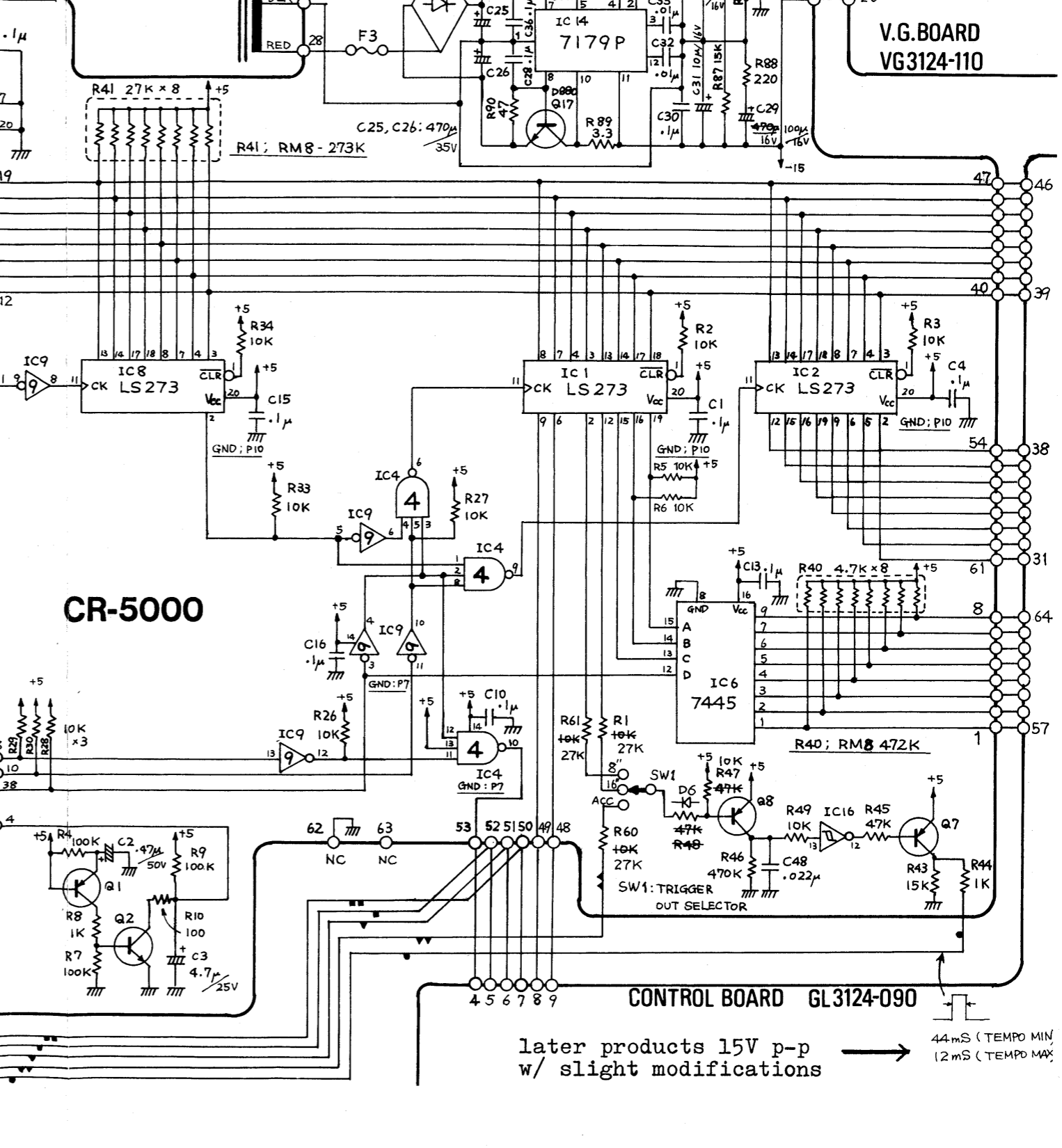
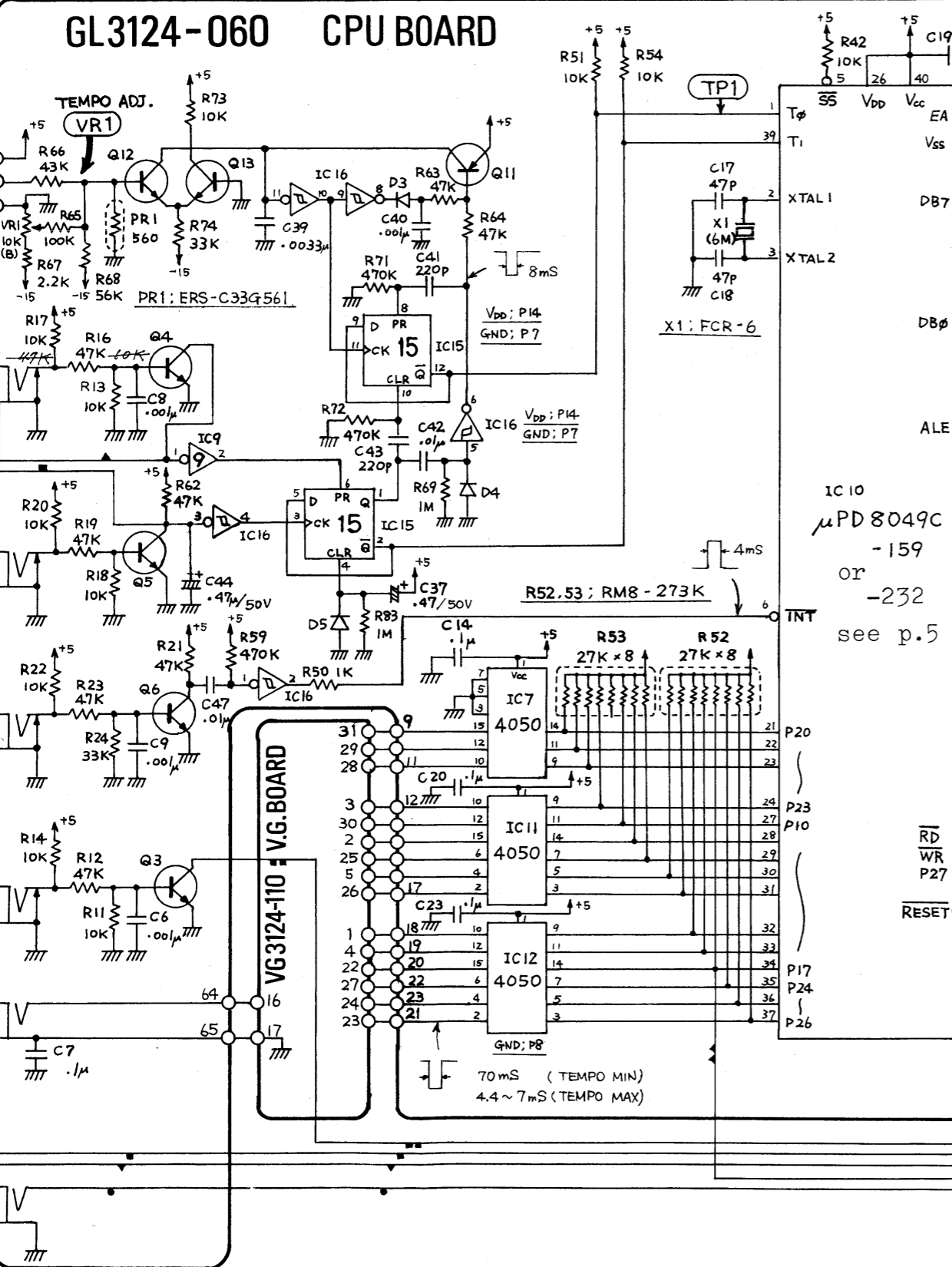
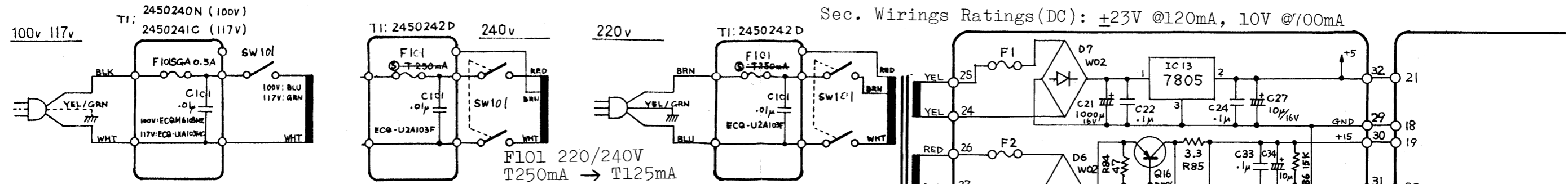


CR-5000 BLOCK DIAGRAM

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42

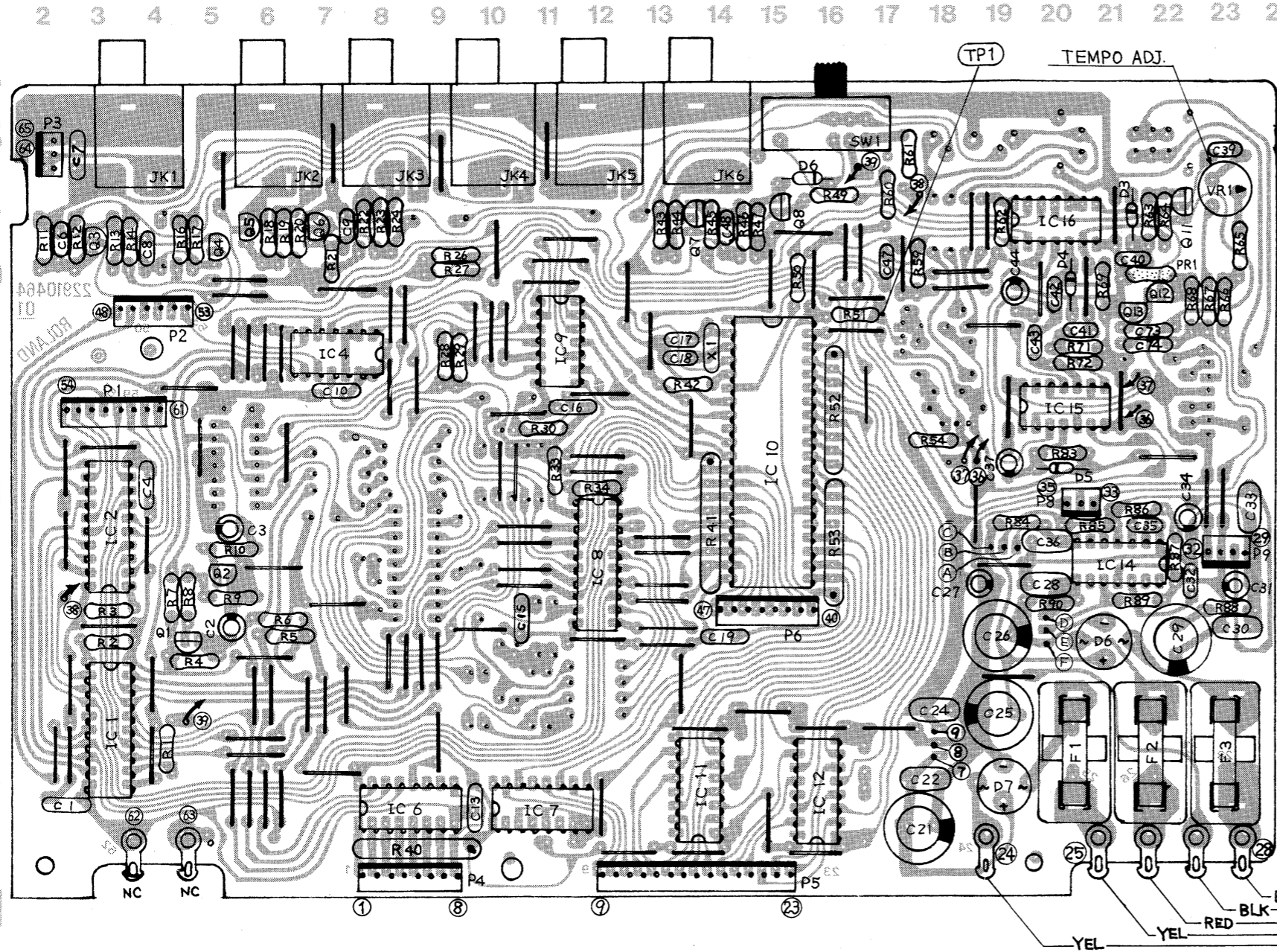
A  
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G  
H  
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J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V

Sec. Wirings Ratings(DC): +23V @120mA, 10V @700mA



later products 15V p-p w/ slight modifications → 44mS (TEMPO MIN) 12mS (TEMPO MAX)

A  
B  
C  
D  
E  
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G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V



- 2SC 945 P
- 2SA 733 P
- DS442 or 1S2473 / 1S1588
- Posistor ERS-C33G561
- Ceramic Resonator
- Resistor Array
- R40, R41, R52, R53
- 0.1µF Ceramic
- 0.1µF Mylar

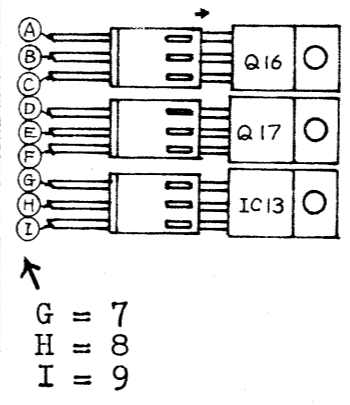
**CR-5000  
CPU BOARD  
GL-3124-060  
(7312406008)  
(pcb 2291046401)**

CHANGES IN COMPONENTS

Ensure trigger outputs at IC1 when low V<sub>OH</sub>

LS273 is used.

R47 47k to 10k  
R48 47k to D6  
R1 10k to 27k  
R61 10k to 27k  
R60 10k to 27k



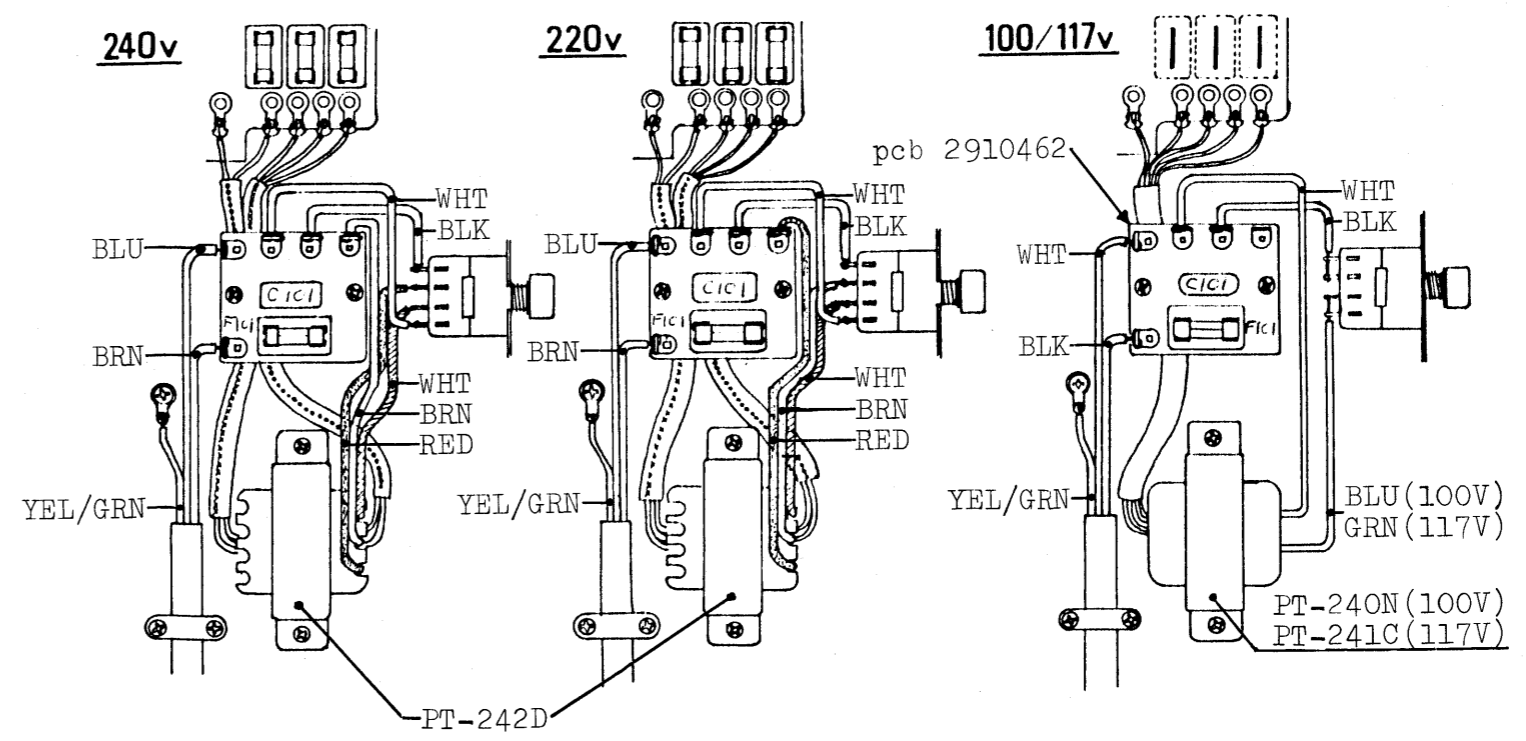
Prevents possible oscillation at final amp upon power off.

C29: 470uF to 100uF

SOME MODIFICATIONS FOR PCB 2291046400 AT FOIL SIDE SEE CR-8000 LAYOUT

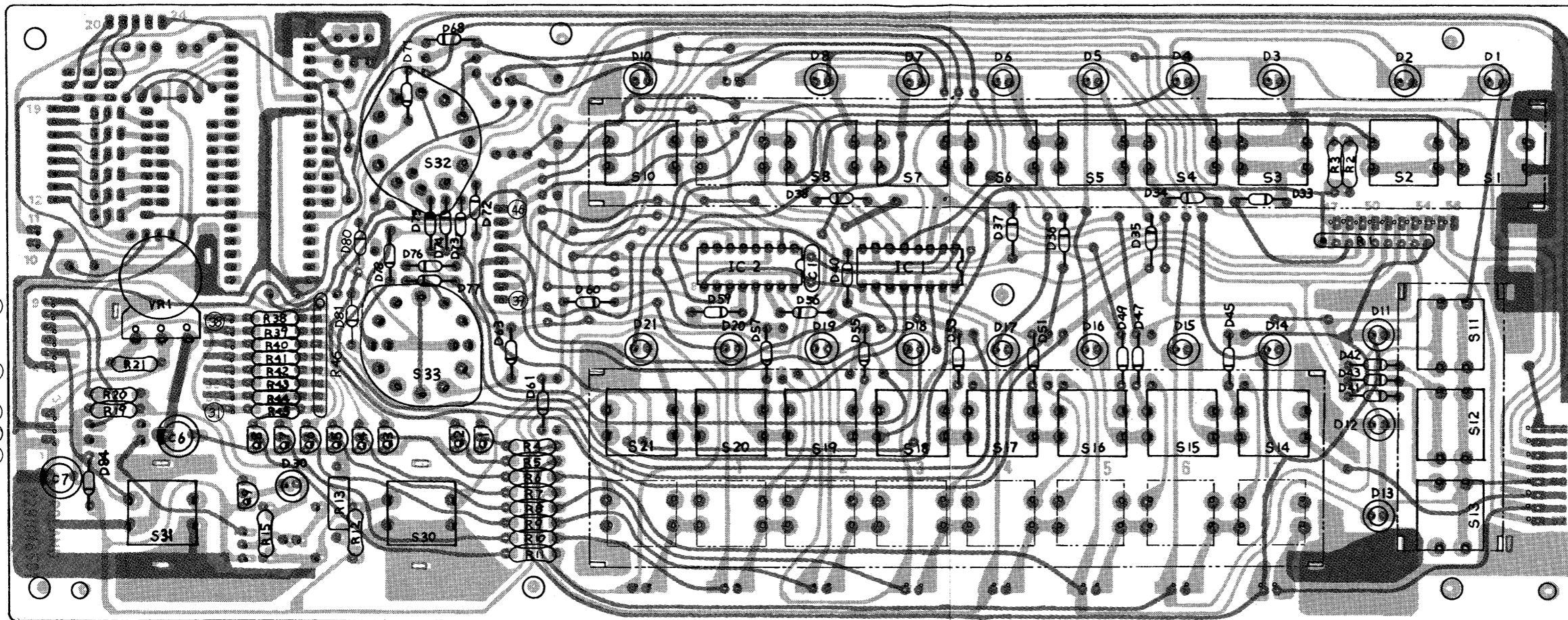
	F1	F2	F3
100V	jumper	jumper	jumper
117V	jumper	jumper	jumper
220v, 240V	CEE T 1A	CEE T 400mA	CEE T 400mA
240V 3P	CEE T 1A	CEE T 400mA	CEE T 400mA

IC1,2,8 ; DM74LS273	IC9 ; HD 74LS04P	Q1,7,8,11 ; 2SA733(P)
IC4 ; HD 14023 BP	D3~5 ; DS 442 or 1S2473 / 1S1588	Q2~6,12,13 ; 2SC945(P)
IC6 ; HD 7445	IC13 ; µA 7805 UC	Q16 ; 2SB596(O)
IC7 ; 11,12 ; HD14050 BP	IC14 ; TA7179 P	Q17 ; 2SD880(Y)
IC15 ; HD14013BP	IC16 ; HD14584BP	

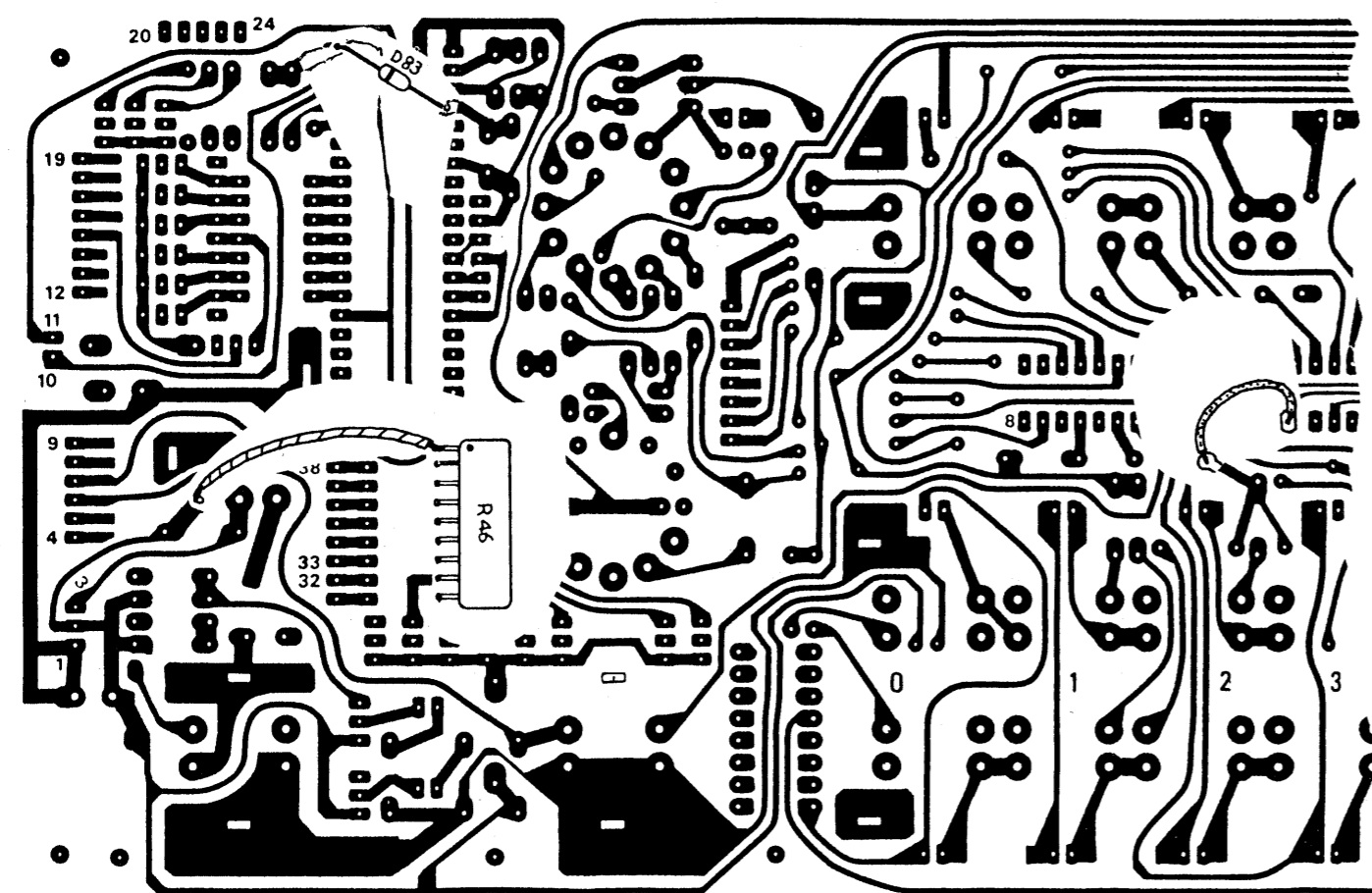





1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V



**CR-5000**  
**CONTROL BOARD**  
**GL3124-090**  
**(7312409010)**  
**(pcb 2291046501)**  
 with serial number 152650  
 (Viewed from the rear)



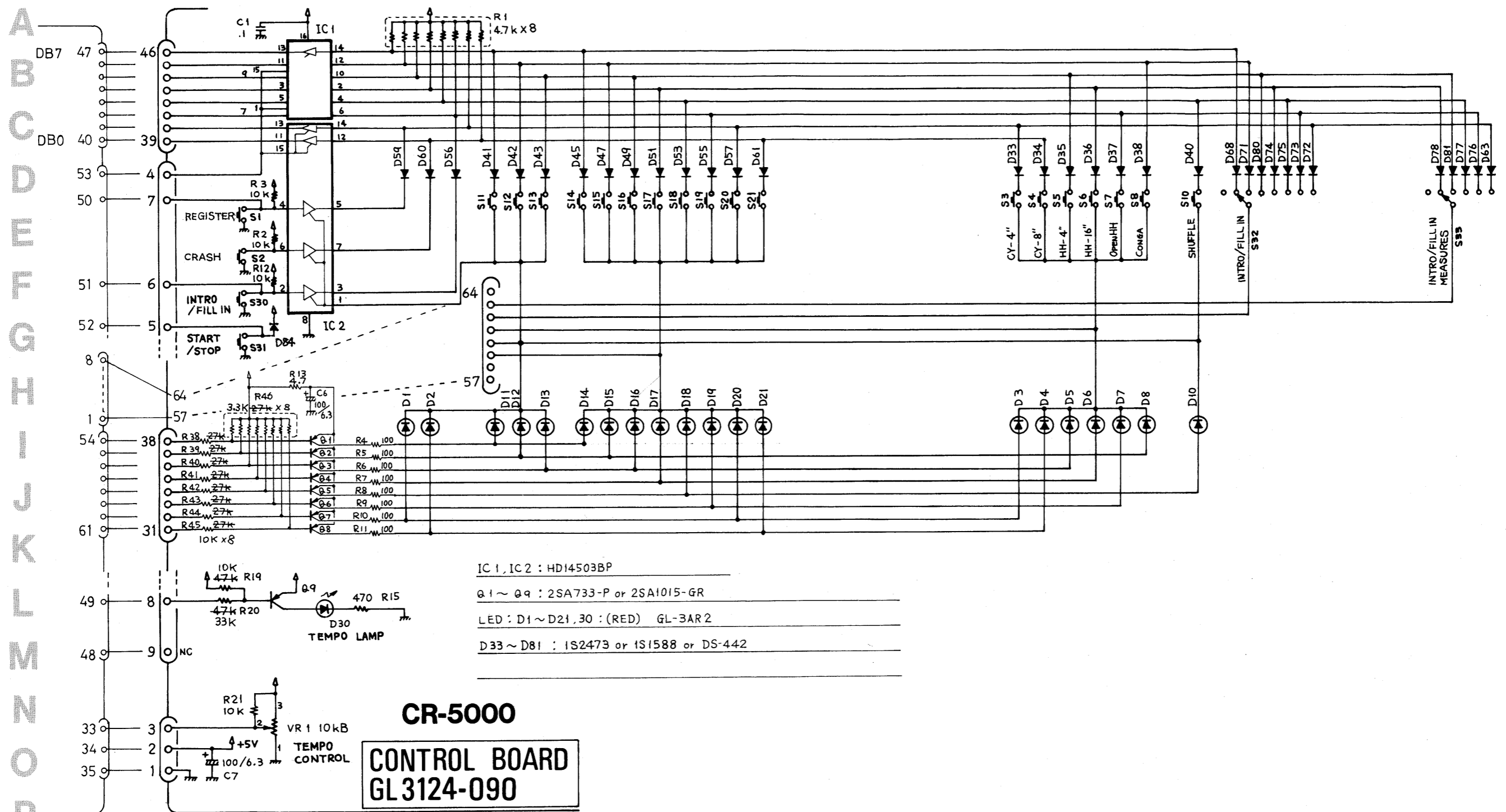
-  : DS442 or 1S1588, 1S2473
-  : 2SA733P or 2SA1015-GR
-  : LED GL-3PR2 (RED)

(pcb 2291046500)

surface mounting  
D83 - CR-8000 only



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40



CPU BOARD

CHANGES IN RESISTANCE With Serial Number 091100 and up  
 The changes eliminates possible dim lighting of LEDs due to insufficient H level output at IC1 or IC2 on CPU board:  
 R38-R45: 27k to 10k      R19: 47k to 10k      R20: 47k to 33k  
 Resistor Array R46: 27k to 3.3k

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

A B C D E F G H I J K L M N O P Q R S T U V

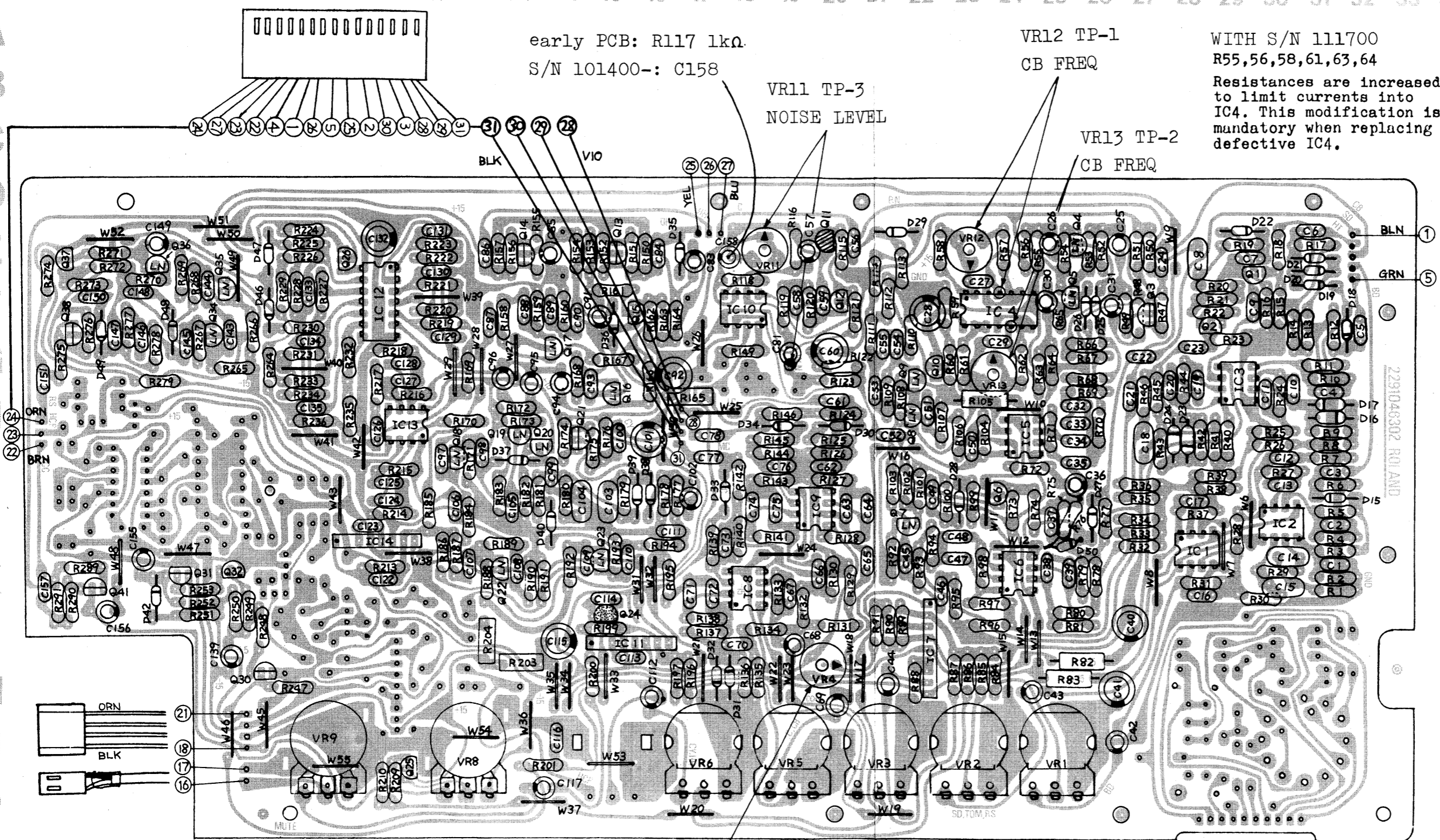
early PCB: R117 1kΩ  
S/N 101400-: C158

VR11 TP-3  
NOISE LEVEL

VR12 TP-1  
CB FREQ

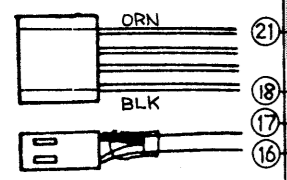
WITH S/N 111700  
R55,56,58,61,63,64  
Resistances are increased  
to limit currents into  
IC4. This modification is  
mandatory when replacing  
defective IC4.

VR13 TP-2  
CB FREQ



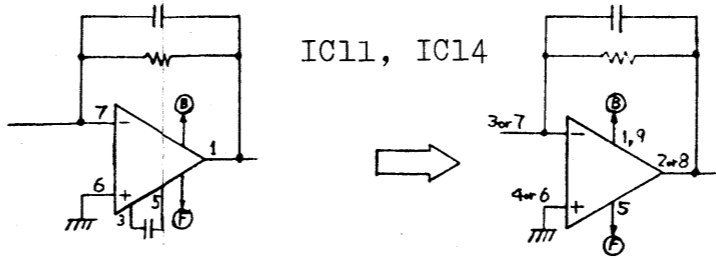
**CHANGES IN COMPONENT WITH SERIAL NUMBERS:**  
**CR-5000 101400**  
**CR-8000 101300**

- SD
  - R94 330 → 2.2k
  - R97 33k → 10k
  - R79 1k → 15k
  - R80 33k → 10k
  - R76 22k → 47k
  - R99 4.7k → 10k
  - R33 33k → 15k
  - R32 33k → 47k
  - R34 33k → 22k
  - R100 2.2M → 1M
  - C48, 47 .033μF → .015μF
  - C39, C38 .027μF → .0047μF
  - C49 .015μF → .018μF
  - C45 .0047μF → .0022μF
  - C46 .001μF → .015μF
- NOISE
  - VR11 5k(B) → 10k(B)
  - R117 1k → open
  - C158 0 → 10μF/16
- TOM TOM
  - R46 6.8k → 22k
  - R38 82k → 33k
  - R39 68k → 27k
  - R37 220k → 82k
  - C18 .068μF → .018μF
  - C7 .01μF → .018μF



VR9 VR8 VR6 VR5 VR3 VR2 VR1

VR4 OFFSET



HA1457W(8-pin) or NJM4558S (9-pin)  
See p. 22 for detail.

View from foil side

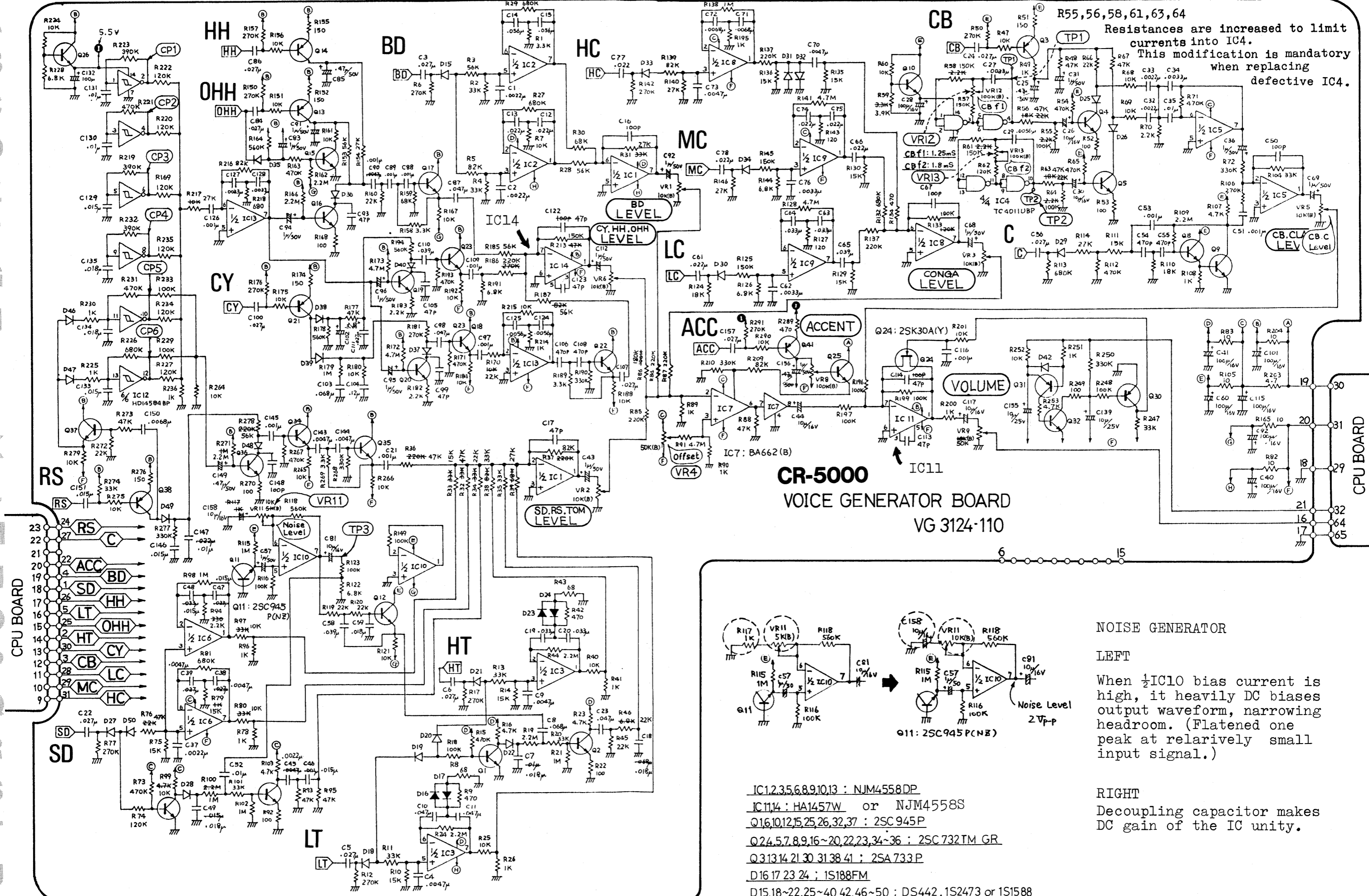
- 2SC945-P
- Ⓛ 2SC732TM-GR
- Ⓜ 2SA733-P
- Ⓢ 2SC945-P(NZ)
- Ⓣ 2SK30A-Y
- Ⓜ DS442, 1S2473 or 1S1588
- Ⓜ 1S188FM

VR9  
with S/N 091100  
From 10k to 50k

**CR-5000**  
**VOICING BOARD**  
**VG3124-110 (7312411009)**  
**(pcb 2291046302)**

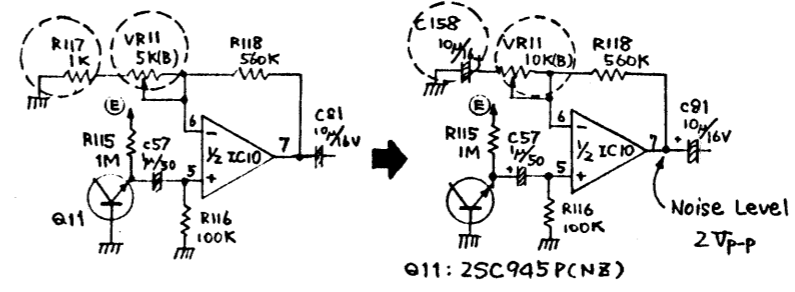
- CY, HH, OHH
  - R217 10k → 27k
  - R170 10k → 22k
  - R187 82k → 56k
  - R186 270k → 220k
  - R213 47k → 150k
  - R86 100k → 180k
  - C90 .0047μF → .001μF
  - C122 100pF → 47pF
- RS
  - R271 1M → 2.2M
  - R278 220k → 56k
  - R36 220k → 47k
  - C147 .002μF → .01μF
- BD
  - R31 33k → 27k
- CONGA
  - R133 120k → 100k
- CB
  - R59 3.3k → 3.9k
  - R56 18k → 22k
  - R63 18k → 22k
- OUTPUT
  - C114 100pF → 47pF
- ACC
  - C156 0.47μF → 1μF

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41



R55,56,58,61,63,64  
Resistances are increased to limit currents into IC4.  
This modification is mandatory when replacing defective IC4.

**CR-5000**  
**VOICE GENERATOR BOARD**  
VG 3124-110



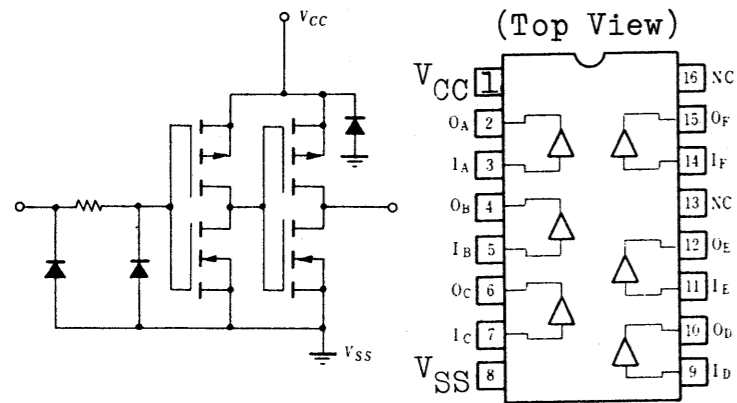
**NOISE GENERATOR**  
LEFT  
When  $\frac{1}{2}$ IC10 bias current is high, it heavily DC biases output waveform, narrowing headroom. (Flattened one peak at relatively small input signal.)  
RIGHT  
Decoupling capacitor makes DC gain of the IC unity.

- IC1,2,3,5,6,8,9,10,13 : NJM4558DP
- IC11,14 : HA1457W or NJM4558S
- Q1,6,10,12,15,25,26,32,37 : 2SC945P
- Q2,4,5,7,8,9,16~20,22,23,34~36 : 2SC732TM GR
- Q3,13,14,21,30,31,38,41 : 2SA733P
- D1,6,17,23,24 : 1S188FM
- D15,18~22,25~40,42,46~50 : DS442, 1S2473 or 1S1588

## PARTS LIST

* CR-8000	** CR-5000	SWITCH	SEMICONDUCTORS
2201061100	Case N-611	13129117 SDK1P power 100V	IC
*2281028102	Chassis(bottom plate) N-281	13129118 SDK1P w/CSA UL 117V	1517911700 $\mu$ PD8049C-159 CPU
*22020159	Battery cover	13129110 ESB-70294 220/240V	or (See Page 5 for difference.)
*12199525	Battery holder	13159316 HSW-0372-01-030 slide	1517913000 $\mu$ PD8049C-323
*2219024802	Holder	TRIG OUT select. SYNC IN/OUT	*15179118 $\mu$ PD8048C-305 CPU display
*2226031000	Cushion	13129714 KEH10903 RHYTHM SELECT	15159105HO HD14013BP
**2281027302	Chassis(bottom plate) N-273	13119508 SRM1026K15 FILL IN MEASURE	15159126HO HD14023BP
2235010100	Rubber foot	*13119806 SRM101CY15 FILIN SELT.INSTMNT	15159128HO HD14050BP
2281027201	Chassis N-272 power trans.	*13159304 SSBO2335 PROGRAM MODE	15159303HO HD14584BP
*2221027100	Panel(upper) N-271	**13119704 SRM1018K15 FILL IN SELECT	15169304HO HD74LS04P
**2221025900	Panel(upper) N-259	PCB	15169325CO DM74LS273N octal D FF
*2221027200	Panel(lower) N-272	*7312506009 CPU (pcb 2291046401)	15169115HO HD7445 BCD-TO-DECIMAL DEC
**2221026000	Panel(lower) N-260	**7312406008 CPU (pcb 2291046401)	*15179305 $\mu$ PD444C RAM
*2222030200	Escutcheon(LED window)N-302	*7312509008 CONTROL (pcb 2291046500)	15199110TO TA7179P $\pm$ 15V regulator1519
		**7312409010 CONTROL (pcb 2291046500)	15199106FO $\mu$ A7805UC +5V regulator
		*7312512007 VOICING (pcb 2291046302)	15159306HC HD14503BP
		**7312411009 VOICING (pcb 2291046302)	15159103TO TC4011UBP
		*7312511001 LED (pcb 2291046600)	15189103 NJM4558DP
		2291046200 FUSE	*15189113 AN6912
		JACK. SOCKET	15189502 HA1457W (pin incompatible, see p. 22)
		13449106 SG7622#8	or NJM4558S
		*13429607 DIN socket TCS0707-01-010	15229803 BA662B VCA
		FUSE	TRANSISTOR
		12559104 SGA 0.500 100/117V	15119105 2SA733P
		12559505 CEE T125mA(s) 220/240V	15129108 2SC945-P
		12559510 T400mA CEE(s) $\pm$ 15V 220/240V	15129108A 2SC945-P(NZ) noise
		12559513 CEE T1A(s) +5V 220/240V	15129104 2SC732TM-GR
		12199519 Fuse clip TF-758	*15119121 2SA937-Q
		RESISTOR ARRAY	*15129121 2SC2021-R
		13910107 RM8-332K 3.3K x 8	15139101 2SK30ATM-Y
		13910101 RM8-472K 4.7K x 8	15119806 2SB596-0 or Y
		13910102 RM8-273K 27K x 8	15129816 2SD880-0 or Y
		POTENTIOMETER	LED
13219229	EVHRRRA361B14 TEMPO, VOLUME on early units		15029109 GL-3AR2 red
13219312	EVHLWAD25B14 Voice level		*15029112 GL-3PG2 green BEAT
13219238	EVHRRRA361B15 ACCENT		*15029125 TLR312 DISPLAY
13219245	EVHRRRA361B54 VOLUME not on early products		Diode
13299106	EVTR4AA00B53 5kB trim		15019107 DS442 or 1S1588 or 1S2473
13299101	EVTR4AA00B14 10kB trim		15019122 1S188FM
13299107	EVTR4AA00B54 50kB trim		15019236 W02 bridge rectifier
13299102	EVTR4AA00B15 100kB trim		12389708 FCR-6 (6.0MHz) ceramic resonator
			15229909 ERS-C33G561 560 ohm posistor

### HD14050B Hex Buffers



### 2SA937 2SC2021



### MC14503B HEX NON-INVERTING 3-STATE BUFFER

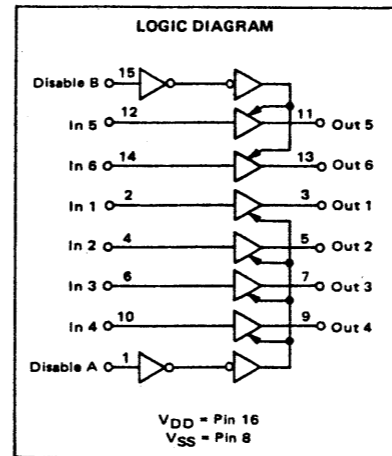
TRUTH TABLE

In <sub>n</sub>	Appropriate Disable Input	Out <sub>n</sub>
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

MAXIMUM RATINGS (Voltages referenced to V<sub>SS</sub>, Pin 8)

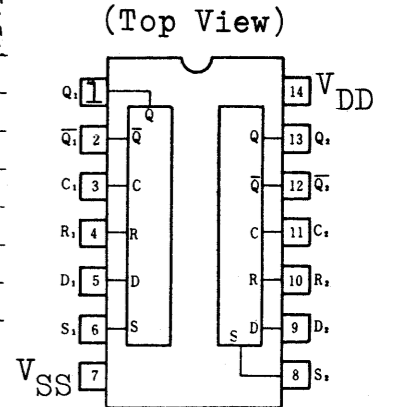
Rating	Symbol	Value	Unit
DC Supply Voltage	V <sub>DD</sub>	-0.5 to +18	V <sub>dc</sub>
Input Voltage, All Inputs	V <sub>in</sub>	-0.5 to V <sub>DD</sub> + 0.5	V <sub>dc</sub>
DC Current Drain per Input Pin	I <sub>i</sub>	10	mAdc
DC Current Drain per Output Pin	I <sub>o</sub>	25	mAdc
Operating Temperature Range - AL Device	T <sub>A</sub>	-55 to +125	°C
	CL/CP Device	-40 to +85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C



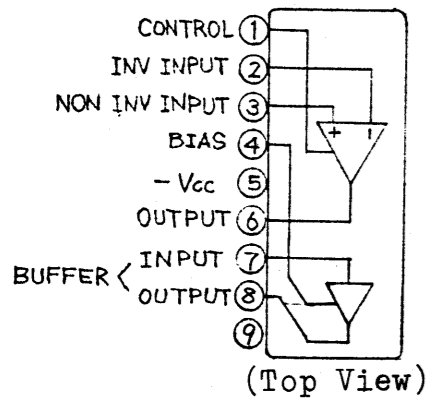
### HD14013B Dual Type D Flip Flop

INPUT OUTPUT

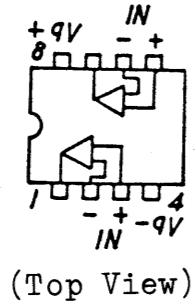
Clock*	Data	Reset	Set	Q	Q̄
0	0	0	0	0	1
1	1	0	0	1	0
X	X	0	0	Q	Q̄
X	X	0	1	1	0
X	X	1	1	1	1



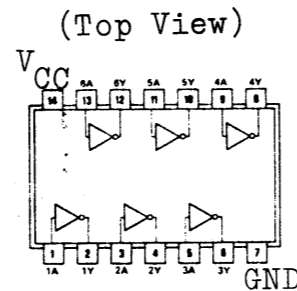
### BA662



### μPC 4558C

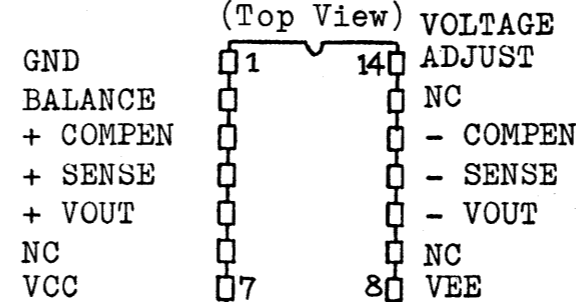


### 74LS04 HEX INVERTER



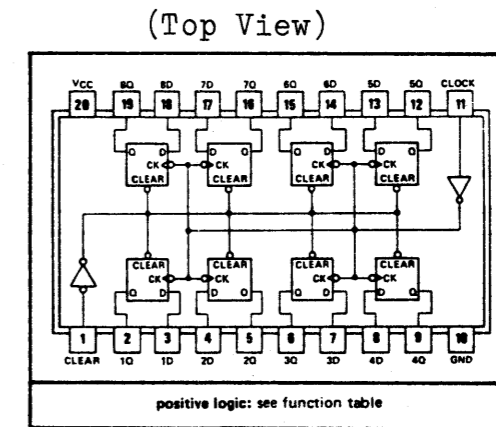
### TA7179P

#### DUAL ±15V TRACKING REGULATOR



Reg. IN = 5mV (typ) (VIN = 18-30V)  
 Reg. OUT = 5mV (typ) (IOUT = 0-50mA)  
 Ripple rejection ratio = 75dB  
 Output current = 100mA (max)

### N74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR



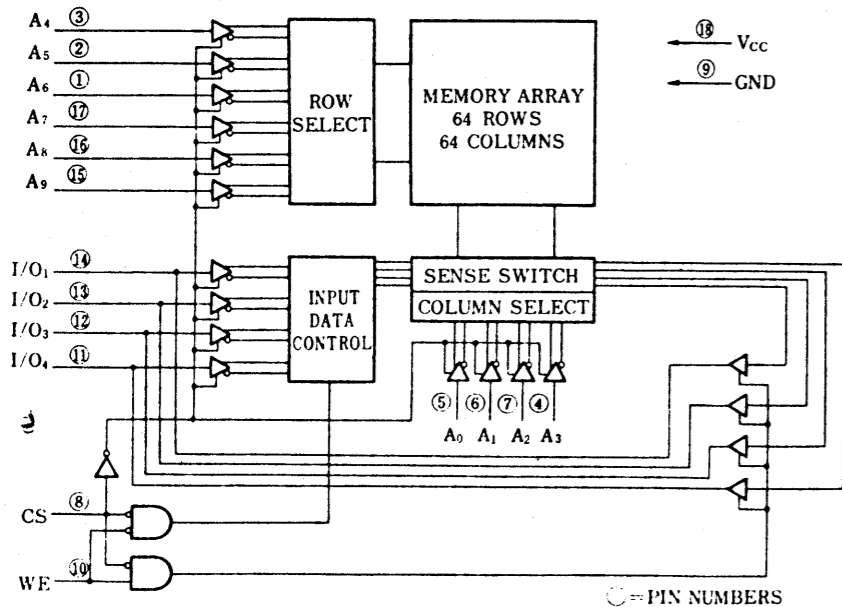
FUNCTION TABLE (EACH FLIP-FLOP)

CLEAR	INPUTS			Q
	CLOCK	D	Q	
L	X	X	L	
H	↑	H	H	
H	↑	L	L	
H	L	X	Q <sub>0</sub>	

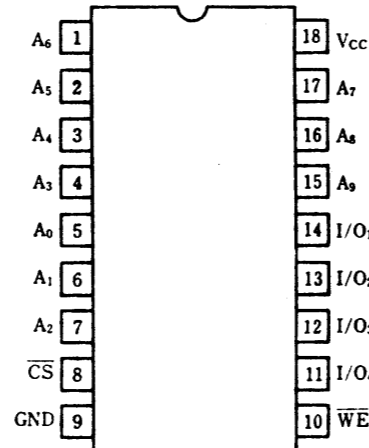
### HM4334P-4

#### μPD444C

#### 4096 BIT STATIC CMOS RAM

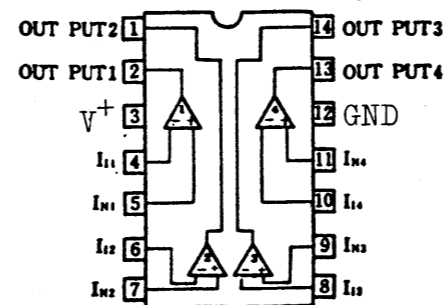


(Top View)

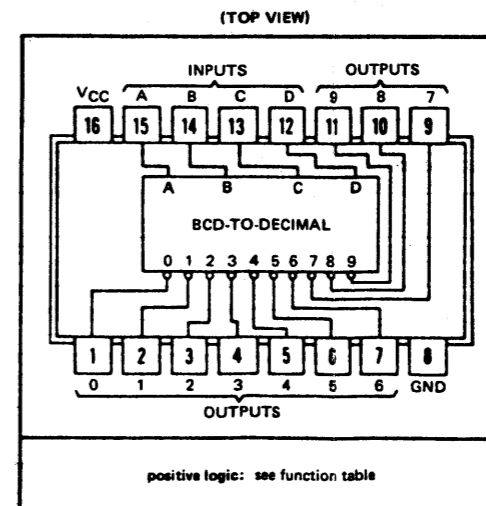


### μPC177C, AN6912 Quad Comparator

Connection Diagram (Top View)



### N7445 BCD-TO-DECIMAL DECODERS/DRIVERS



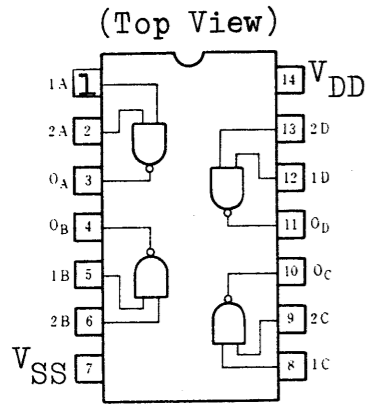
FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	H	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	H	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	H	H	H	H	H	H
5	L	H	L	H	L	L	H	H	H	H	L	H	H	H
6	L	H	H	L	L	L	H	H	H	H	L	L	H	H
7	L	H	H	H	L	L	L	H	H	H	L	L	L	H
8	H	L	L	L	L	L	L	L	L	L	L	L	L	H
9	H	L	L	H	L	L	L	L	L	L	L	L	L	L
INVALID	H	L	L	H	L	L	L	L	L	L	L	L	L	L
	H	L	H	L	L	L	L	L	L	L	L	L	L	L
	H	L	H	H	L	L	L	L	L	L	L	L	L	L
	H	H	L	L	L	L	L	L	L	L	L	L	L	L

H = high level (off), L = low level (on)

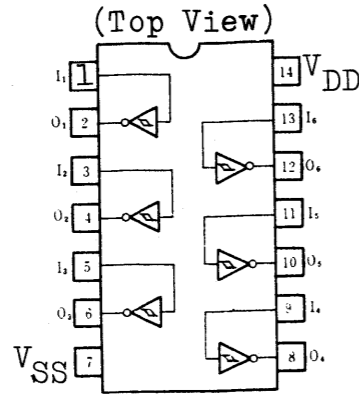
**HD14011B**

Quadruple 2-input NAND Gate



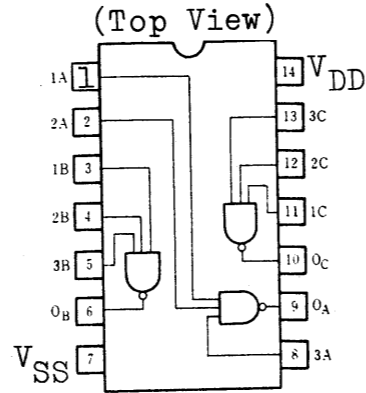
**HD14584B**

Hex Schmitt Trigger



**HD14023B**

Triple 3-input NAND Gate



CHANGING OPERATIONAL AMPLIFIERS

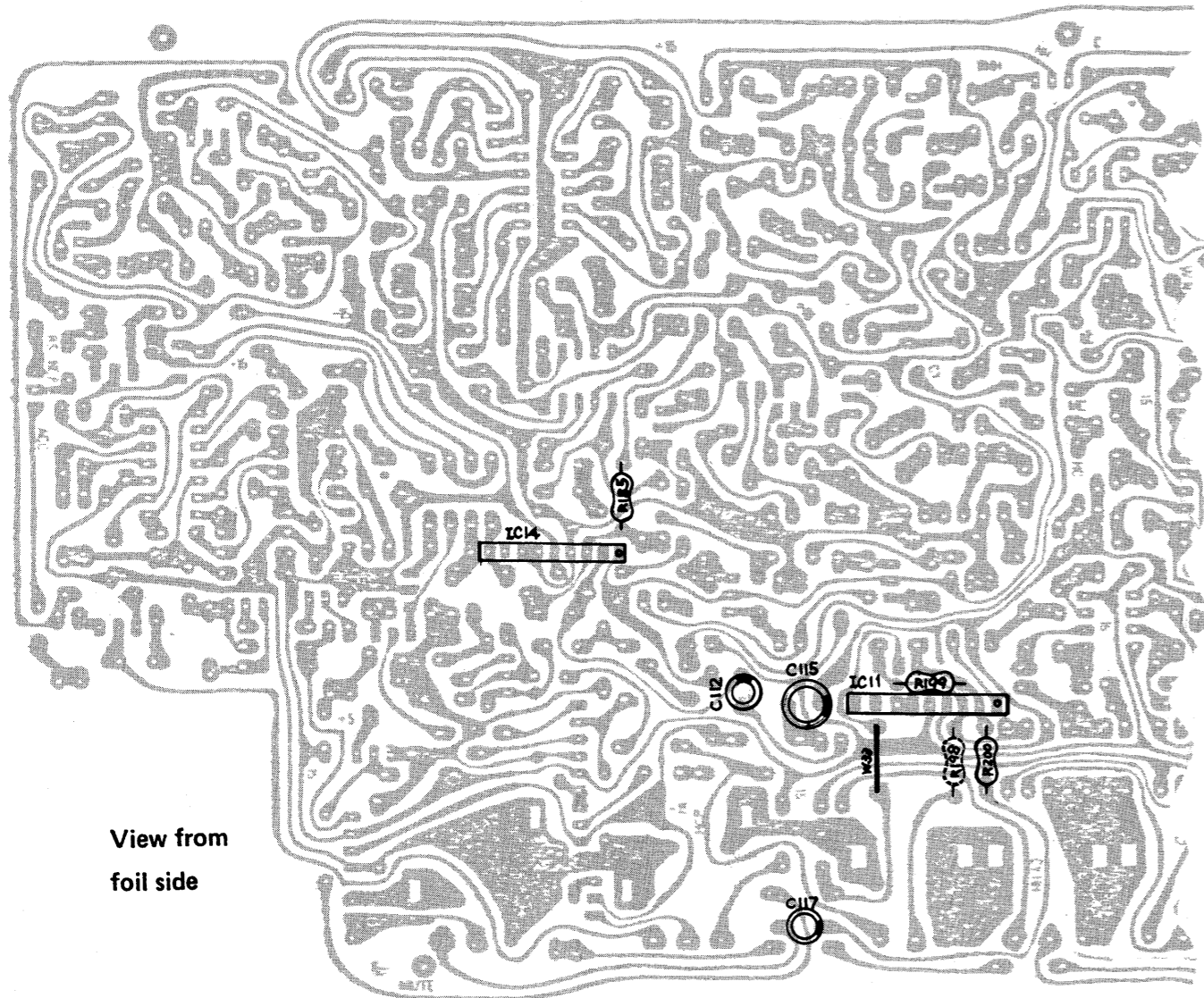
On CR-5000/8000 VG Boards as well as in other Roland products, the IC NJM4558S replaces HA1457W which is discontinued at the semiconductor manufacturer.

Incompatible pin arrangement leads to minor PCB re-layout as shown below, which is due to put into practical production.

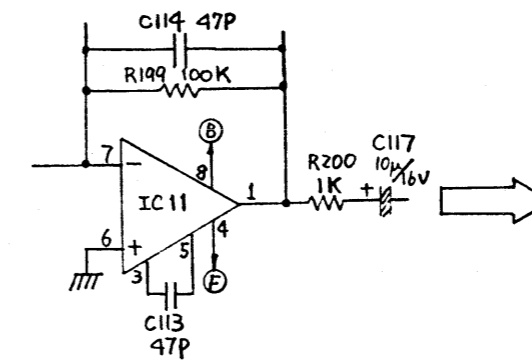
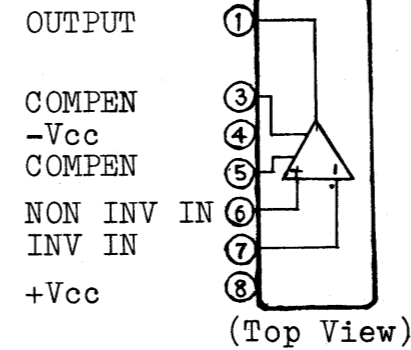
Serial Numbers with which the change is effective on the CR-5000/8000 are not fixed as of the date this edition is closed.

NOTE: Although two OP AMPs are contained in new IC, one is left redundant in this application.

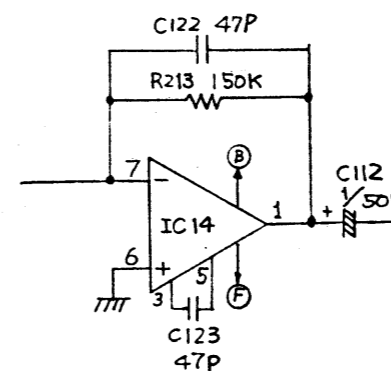
**VOICING BOARD CHANGES**



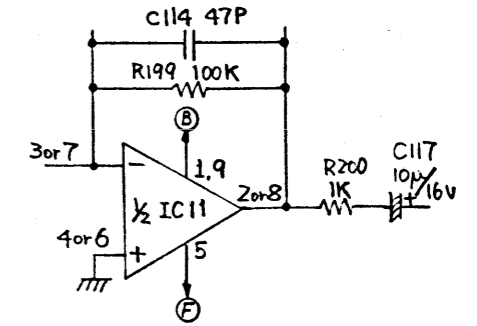
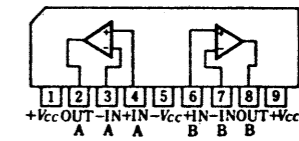
**HA1457W**



**HA1457W**



**NJM4558S**



**NJM4558S**

