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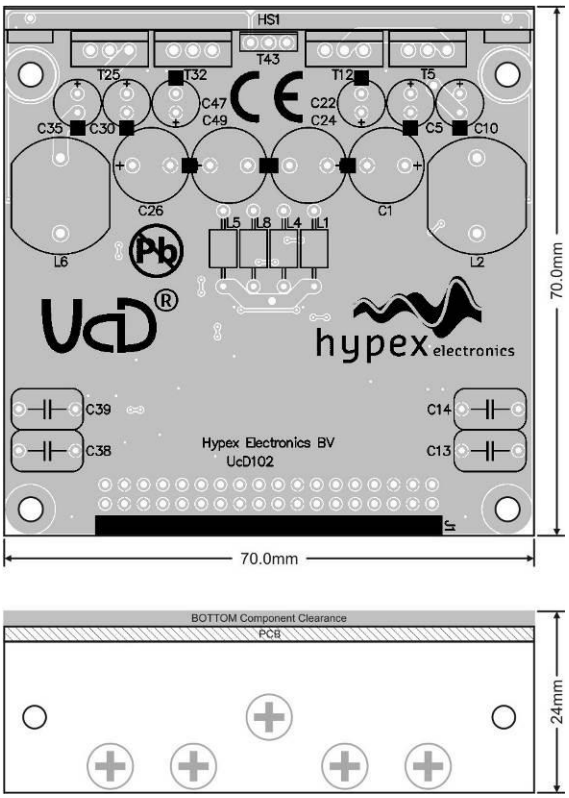
UcD102

Dual Channel High Efficiency Power Amplifier Module



Highlights

- Flat, fully load-independent frequency response
- Low output impedance
- Very low, frequency-independent THD
- Very low noise
- Fully passive loop control
- Consistent top performer in listening trials

Features

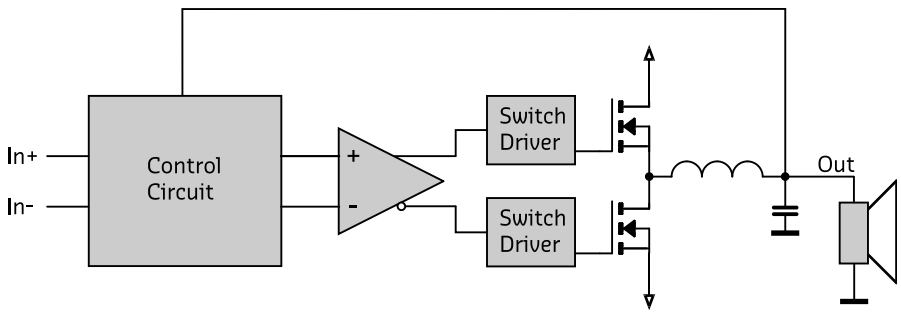
- Runs on unregulated +/- rails
- Pop-free start and stop control
- Differential audio input
- DC-fault detection
- Overcurrent protection
- Weight: 55 g / Height: 24mm

Applications

- Monitor loudspeakers for recording and mastering studios
- Audiophile power amplifiers for professional and consumer use
- Public Address systems
- Home theatre systems
- Active loudspeakers

Description

The UcD102 amplifier module is a dual channel self-contained high-performance class D amplifier intended for a wide range of audio applications, ranging from Public Address systems to ultrahigh-fidelity replay systems for studio and home use. Chief distinguishing features are flat frequency response irrespective of load impedance, nearly frequency-independent distortion behaviour and very low radiated and conducted EMI. Control is based on a phase-shift controlled self-oscillating loop taking feedback only at the speaker output.



Contents

1 Performance data

Power supply = +/-35V, Load=4Ω, MBW=40kHz, Source imp=40Ω ,unless otherwise noted

Item	Symbol	Min	Typ	Max	Unit	Notes
Max Output Power	P_R 2Ω	-	60	-	W_{rms}	THD=1%
	P_R 4Ω	-	100	-	W_{rms}	
	P_R 8Ω	-	60	-	W_{rms}	
Distortion	THD+N	-	0.03	0.05	%	20Hz<f<20kHz. Pout<P_R/2
		-	-	0.03	%	20Hz<f<20kHz Pout=1W
Output noise	U_N	-	17	25	µV	Unwtd, 20Hz-20kHz
Output Impedance	Z_{OUT}	-	-	22	mΩ	f<1kHz
		-	-	90	mΩ	f<20kHz
Power Bandwidth	PBW		20-35k		Hz	
Frequency Response		DC	-	48k	Hz	+0/-3dB. All loads.
Voltage Gain total	A_V	13.3	13.5	13.7	dB	
Supply Ripple Rejection	PSRR	60	65	-	dB	Either rail, f<1kHz.
Required input level for 100W/4Ω			4.25		V	Appropriate supply voltage assumed
Efficiency	η		92		%	Full power
Idle Losses	P_0	-	4	4.5	W	External VDR
		-	6	7		Internal VDR
Standby Current	I_{STBY}	-	5	7	mA	Positive rail
		-	9	12		Negative rail
Current Limit		6	8		A	

2 Audio Input Characteristics

Item	Symbol	Min	Typ	Max	Unit	Notes
Input Impedance	Z_{IN}		1.8k		Ω	Either input to ground
CM Rejection Ratio	CMRR		55		dB	All frequencies

3 Absolute maximum ratings

Correct operation at these limits is not guaranteed. Operation beyond these limits may result in irreversible damage.

Item	Symbol	Rating	Unit	Notes
Power supply voltage	V_B	+/-48	V	Shuts down when either rail exceeds 50V
Peak output current	$I_{OUT,P}$	8	A	Unit current-limits at 8A
Input voltage	V_{IN}	+/-12	V	Either input referred to ground
Air Temperature	T_{AMB}	55	ºC	
Heat-sink temperature	T_{SINK}	90	ºC	User to select heat sink to insure this condition under most adverse use case

4 Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Notes
Power supply voltage	V_B	20[1)]	36	42[2)]	V	
Load impedance	Z_{LOAD}	1			Ω	
Source impedance	Z_{SRC}			100	Ω	
Effective power supply storage capacitance	C_{SUP}	4700µ[3)]			F	Per rail, per attached amplifier. 4Ω load presumed.

Note 1: Reduced performance.
Note 2: Unit shuts down when either rail exceeds 50V.
Note 3: The effective power supply storage capacitance of Hypex SMPS is already in excess of 4700µF. Do not add supplementary capacitance.

5 Connections

In order to ease connecting the amplifier, all necessary connections to operate the amplifier are grouped in one standard 2.54mm pitch dual row 18 pin header.

Pin	Type	Function
1,2	Output	CH1 Loudspeaker connection (hot)
3,4	Output	CH1 Loudspeaker connection (cold) [1)]
5	Input	CH1 Audio input ground connection[1)]
6	Input	CH1 Inverting audio input
7	Input	CH1 Non-inverting audio input
15,16,22	Input	Power supply ground connection[1)]
17,18	Input	Positive power supply connection
19,20	Input	Negative power supply connection
21	Input	Driver voltage, connect to GND or to external driver voltage[2)]
27	Input	ON/OFF control (Active low)
28	Output	DC-fault detection (Open collector - Active low)
30	Input	CH2 Non-inverting audio input
31	Input	CH2 Inverting audio input
32	Input	CH2 Audio input ground connection[1)]
33,34	Output	CH2 Loudspeaker connection (cold) [1)]
35,36	Output	CH2 Loudspeaker connection (hot)

Note 1: Pin 3, 4, 5, 15, 16, 22, 32, 33 and 34 are physically connected to the same potential (ground).
Note 2: Dissipation in the UcD102 can be lowered by using external driver voltage other than GND, see section 5.5 for additional info.

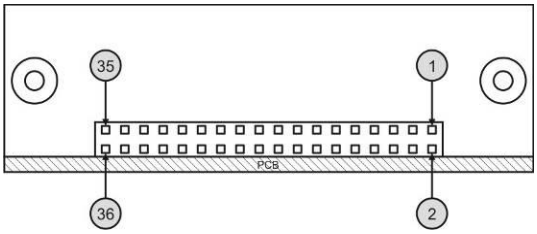


Figure 1. Connector pinning UcD102

5.1 DC-Error Detection Characteristics

The UcD102 has an integrated DC-error detection which will pull pin 28 low in case of such an event. It is recommended to sense this fault condition and to interrupt both power supply lines in such an event.

Item	Type	Min	Typ	Max	Unit	Notes
Voltage on pin 28, DC-error	Output			1	V	Internal open collector[1)]

Note 1: Must be pulled to a positive voltage by means of an external resistor. Open collector maximum output current: 100mA. Maximum collector voltage: 65V.

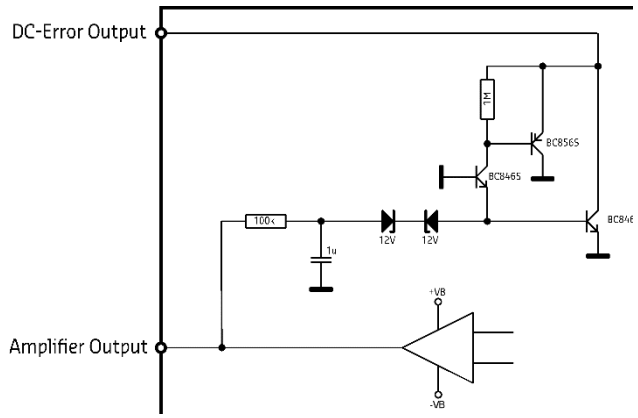


Figure 2. DC-Error Output interface.

5.2 Amplifier On/OFF Characteristics

Pulling pin 27 low enables the amplifier. Leaving pin 27 floating will put the amplifier in standby. This pin may be driven from a logical output or an open collector.

Item	Min	Typ	Max	Unit	Notes
Voltage on pin 27, left floating			3	V	Internally pulled up
Pull-up current	20		40	uA	
Threshold voltage	1.8	2.2	2.7	V	
Permissible voltage range	-5	-	75	V	

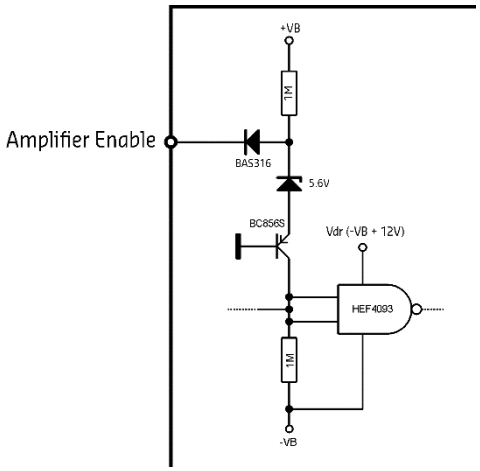


Figure 3. Amplifier On/Off Control interface.

5.3 Input buffer recommendation

The UcD102 has no on-board input buffer. Applications that require a higher gain and/or a higher input impedance benefit from a buffer stage like shown below.

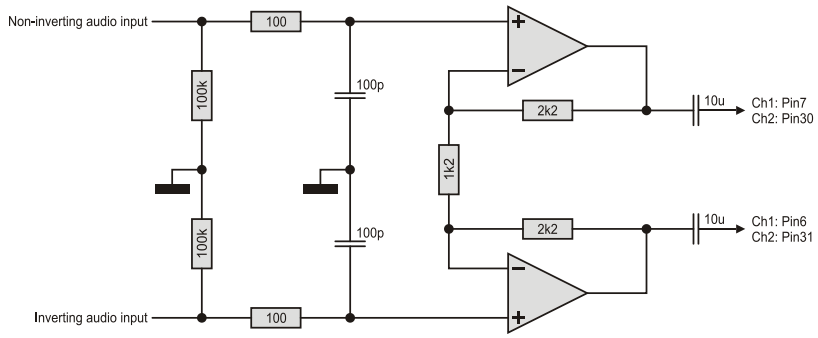


Figure 4. Recommended Input buffer stage.

5.4 Amplifier start-up delay

During initial power up the amplifier is disabled for approx. 1.5s regardless of the state of pin 27. Once powered up there is no start or stop delay.

5.5 External Driver Voltage Connection

An internal linear VDR regulator is available. In order to minimize dissipation in multi-channel applications an external voltage source can be connected. The VDR reference must be connected to the negative supply rails(!). Driver current is independent of driver voltage, regulator losses increase linear with applied voltage. If no external VDR is available the input should be connected to GND in order for the UcD102 to operate.

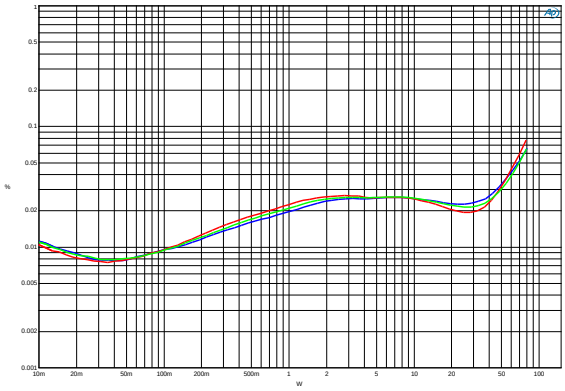
Item	Min	Typ	Max	Unit	Notes
External driver voltage	13	-	GND	V	1)
Driver current amp muted	-	8		mA	
Driver current	-	85		mA	

Note 1: This voltage is in respect to the negative supply rails, if no external driver voltage is available, connect to GND

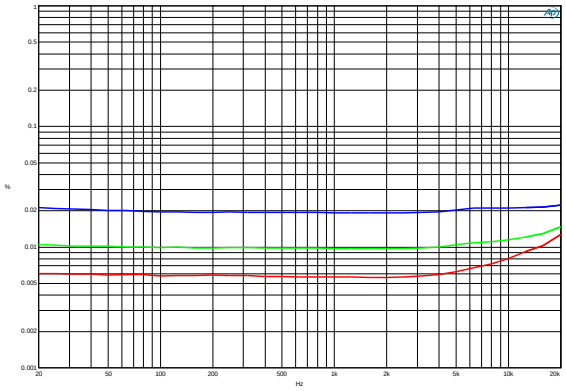
6 Typical Performance Graphs

The graphs were taken on one stock UcD102 module powered by an SMPS400A100. Refer to the tables in section 1 for guaranteed limits.

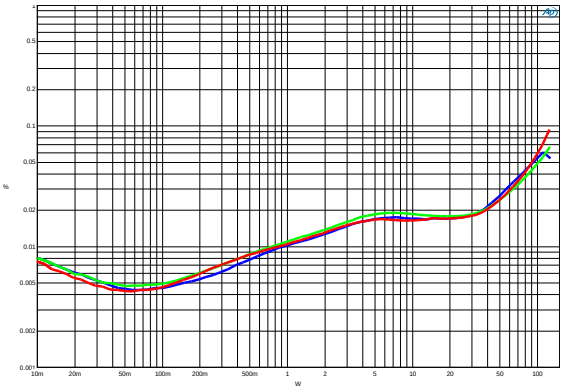
6.1 THD+N over power and frequency



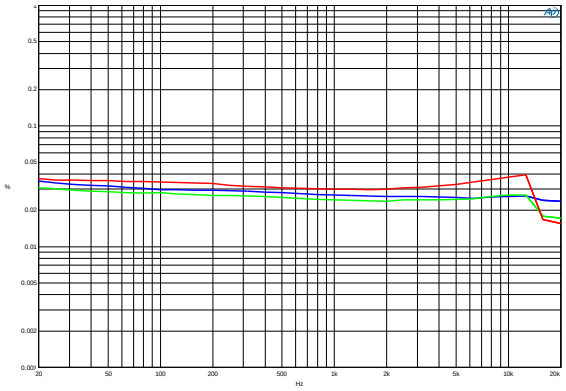
THD+N vs. power at 100Hz (blue), 1kHz (green) and 6kHz (red) (2Ω).



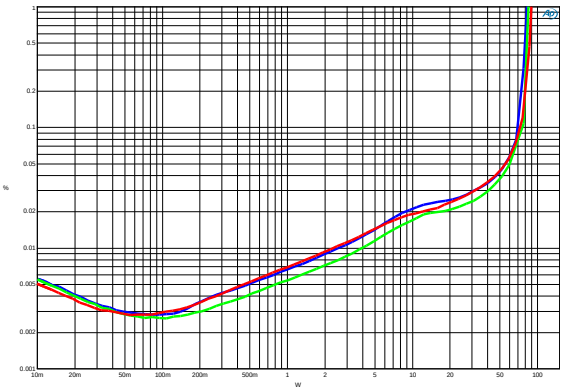
THD+N vs. Frequency at 1W in 2Ω (blue), 4Ω (green) and 8Ω (red).



THD+N vs. power at 100Hz (blue), 1kHz (green) and 6kHz (red) (4Ω).

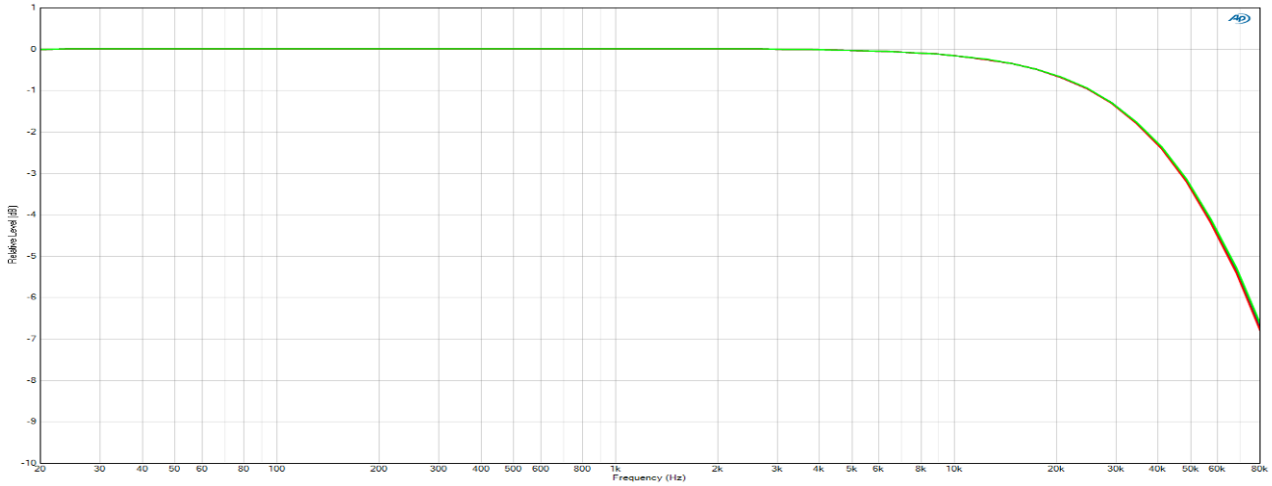


THD+N vs. Frequency at $P_R/2$ in 2Ω (blue), 4Ω (green) and 8Ω (red).

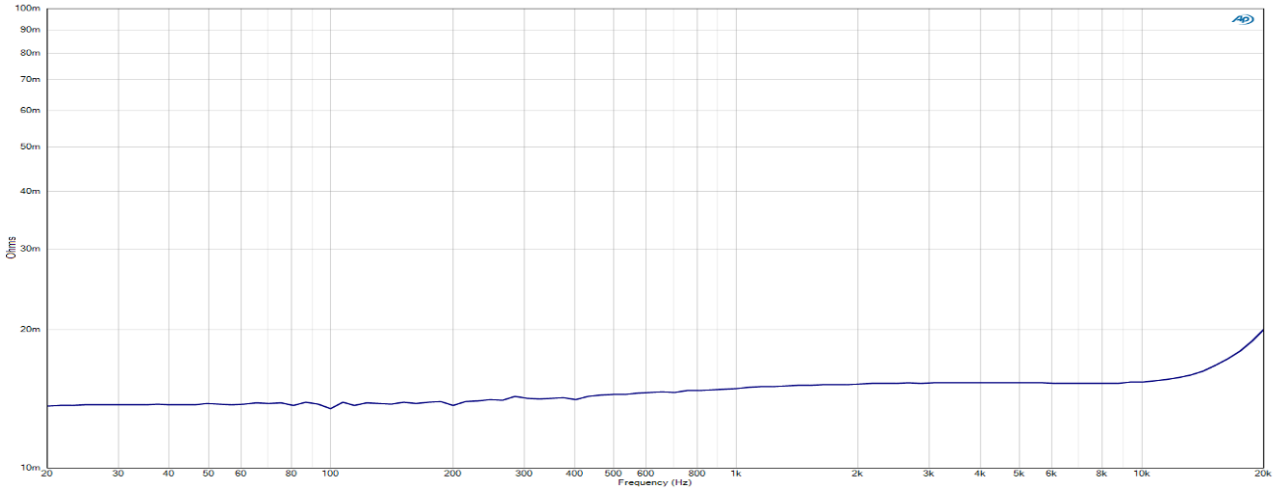


THD+N vs. power at 100Hz (blue), 1kHz (green) and 6kHz (red) (8Ω).

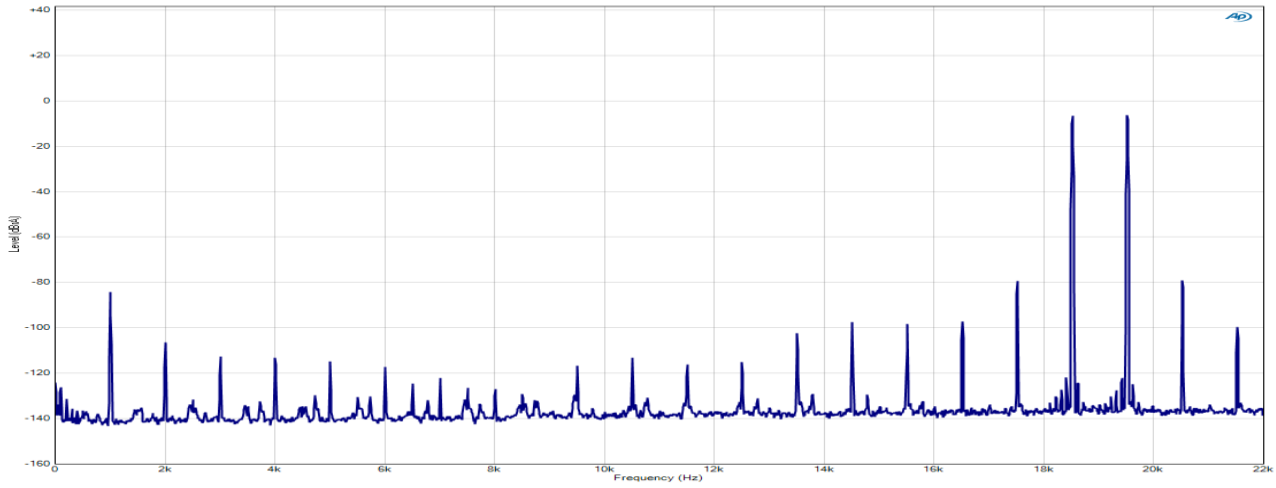
6.2 Frequency Response (4Ω, 8Ω and open circuit)



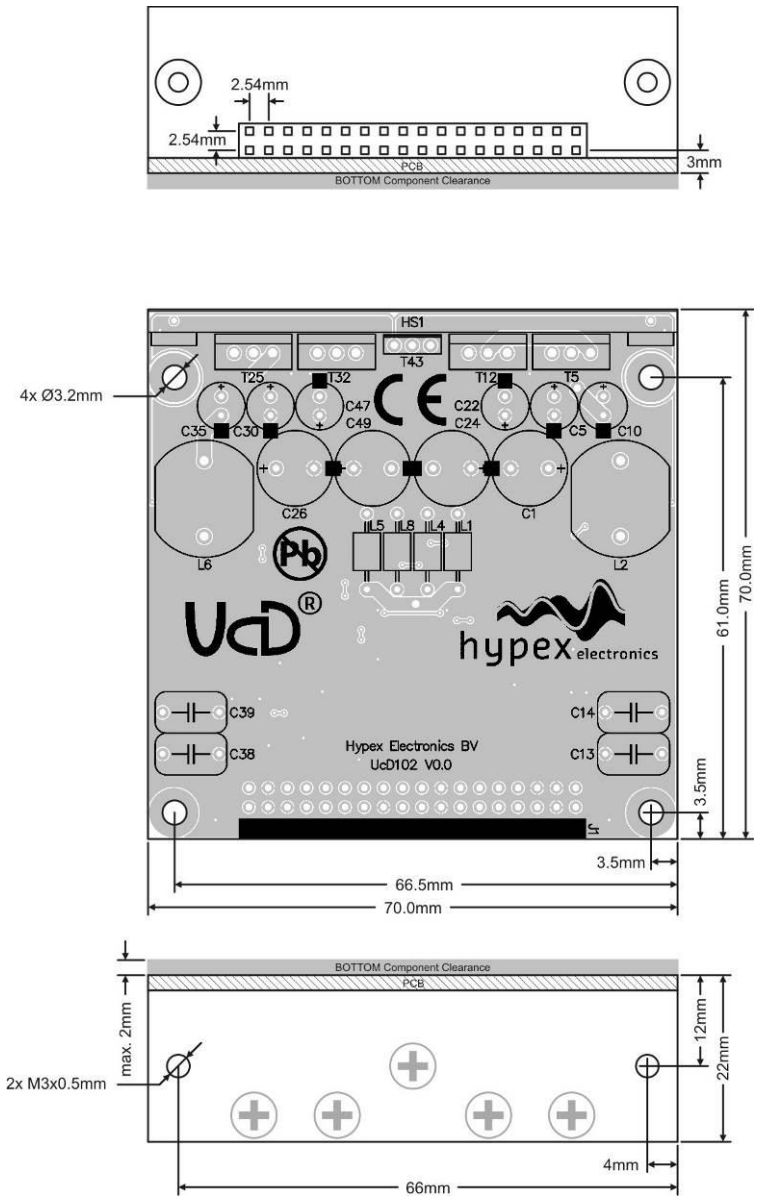
6.3 Output Impedance



6.4 18,5+19,5kHz IMD (10W, 8Ω)

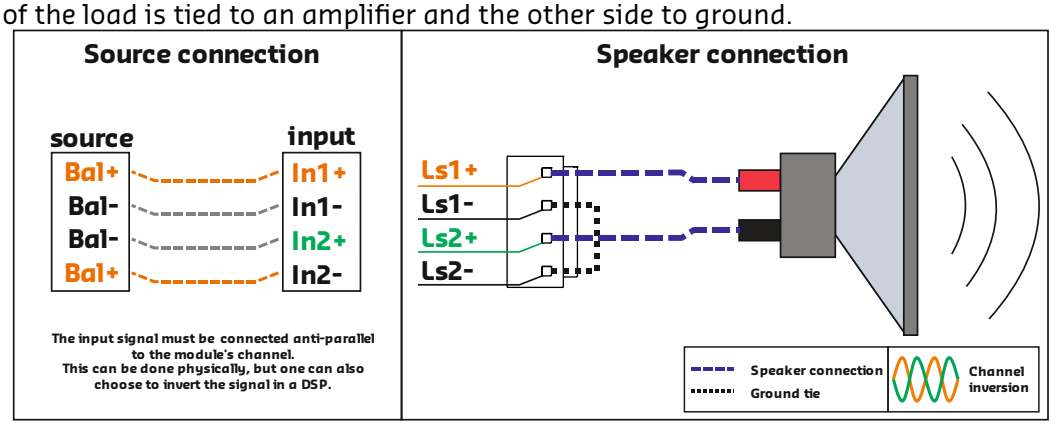


7 Mechanical Dimensions



8 Bridge-tied load (BTL)

This two channel amplifier can be utilized in Bridge Tied Load configuration. This is especially useful for high impedance loads. In a bridge-tied load configuration, channel 1 is driving one side of a load and channel 2 is driving the other side of the load. The signal input of channel 2 is the inverted signal input of channel 1. Note that this does not affect the phase of the signal. A BTL configuration results in double the voltage swing across the load compared to a single-ended configuration where one side of the load is tied to an amplifier and the other side to ground.

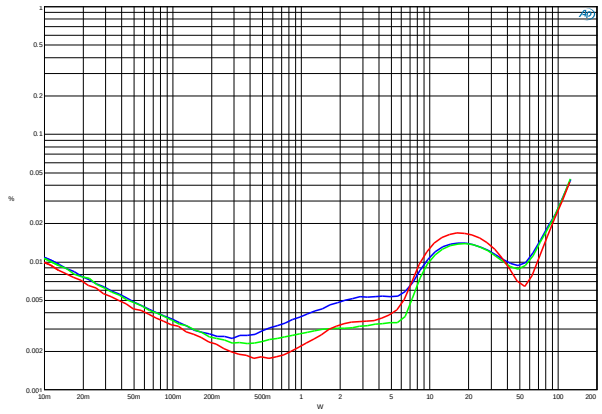


In the graphical representation above, the BTL principle is depicted. By inverting the signal input of the second channel, the output voltage amplitude is doubled. Please note that the negative (GND) output terminals are tied together. On the UcD102 module, this is already implemented in the design and therefor these pins can be left unconnected.

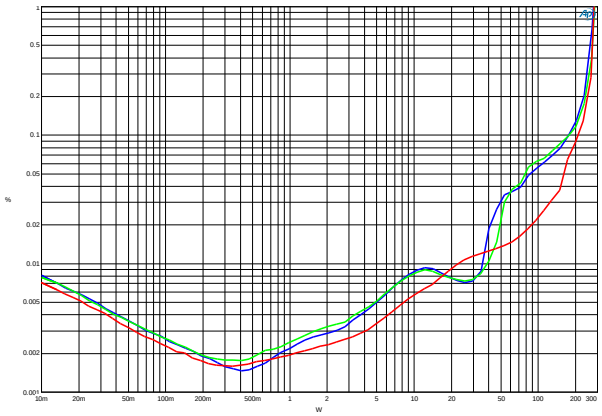
In a bridge-tied load configuration, the load impedance which each amplifier channel 'sees' is half the characteristic impedance of the connected speaker. Therefor the minimum load in BTL configuration is 4Ω, however, we recommend to use only a BTL configuration with a load of 8Ω or higher.

Parameter	Remarks	Symbol	Min	Typ	Max	Unit
Max Output Power	1KHz, THD=1%, Bridge-tied load (BTL)	$P_{R,\ 4\Omega}$	-	-	100	Wrms
		$P_{R,\ 8\Omega}$	-	-	200	Wrms
Voltage Gain	Bridge-tied load (BTL)	A_V	19	19.5	20	dB
Loudspeaker impedance range	Bridge-tied load (BTL)	$Z_{L,SE}$	4	8	-	Ω

8.1 Typical Performance Graphs BTL



THD+N vs. power at 100Hz (blue), 1kHz (green) and 6kHz (red) (BTL - 4Ω).



THD+N vs. power at 100Hz (blue), 1kHz (green) and 6kHz (red) (BTL - 8Ω).

DISCLAIMER: This subassembly is designed for use in music reproduction equipment only. No representations are made as to fitness for other uses. Except where noted otherwise any specifications given pertain to this subassembly only. Responsibility for verifying the performance, safety, reliability and compliance with legal standards of end products using this subassembly falls to the manufacturer of said end product.

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Document Revision	PCB Version	Description	Date
R1	UcD102 V0.0	Initial Draft.	30.05.2012
R2	UcD102 V0.3	Performance Graphs added	04.02.2013
R3	UcD102 V1.0	Performance Graphs added for 2Ω, 8Ω and BTL Added VDR info	01.05.2020